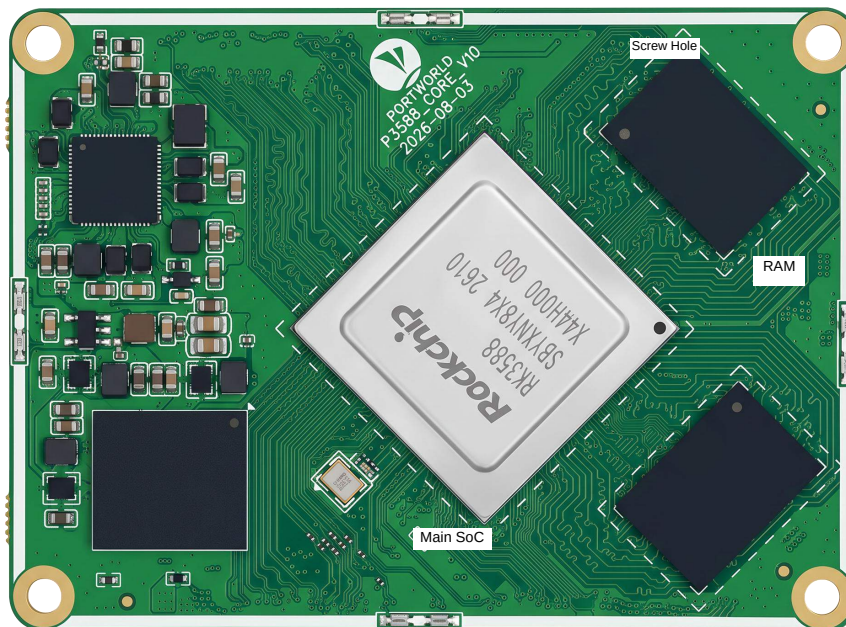




P3588 CORE V10 Core Module Hardware Specification



Product Model	P3588_CORE_V10
Board Silkscreen	PORTWORLD P3588_CORE_V10 2026-08-03
Document Version	V1.1
Release Date	2026-09-10
Compatible Carrier Board	YC Development Carrier Board
Document Status	Official Release

This document describes the hardware resources, mechanical and electrical specifications, interface definitions and carrier-board compatibility limits of P3588_CORE_V10.

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Technical Service Support

1. Documentation and Services

- Product documentation is subject to the supplied documentation package, software release package and controlled hardware files.
- Hardware support covers resource descriptions, connector definitions, interface operating conditions and basic integration issues.
- Support for custom carriers, third-party peripherals, device-tree changes and further software development is subject to project agreements.
- Returns, repairs and warranty terms are governed by the service terms of the actual purchase channel.

2. Customization Services

Customization of RAM, eMMC, connectors, temperature grade, software features and carrier integration requires confirmation of technical feasibility and delivery scope during project evaluation. Configurations absent from the order or commercial documents are not standard supply.

3. Disclaimer

This document describes P3588_CORE_V10 hardware and system integration; it does not guarantee final-system performance, environmental suitability or third-party compatibility. Before carrier design, device-tree changes or connecting external devices, verify the latest schematics, netlist, BOM and software release notes.

Manual Revision History

Version	Date	Change Description
V1.0	2026-09-10	Initial release, based on P3588_CORE_V10 schematics, netlist and silkscreen dated 2026-08-03.
V1.1	2026-09-10	Added carrier specifications, operating instructions, reference power data and a more complete manual structure.

Document Scope

- Describes core-module hardware resources, system performance, electrical parameters, mechanical dimensions and interface capabilities.
- Provides J1-J4 pin indexes, counts and references to the companion pin-multiplexing spreadsheet.
- Explains carrier compatibility limits, software support scope and hardware design precautions.
- The companion Excel file is the detailed source for pin multiplexing, default carrier usage and complete alternate functions.

Source Documents

Document	Purpose
P3588_CORE_V10 Schematics	Verify power, clock, reset, boot and interface topology
P3588_CORE_V10 Netlist	Verify J1-J4 pins, nets and default functions
P3588_CORE_V10_Pin_Multiplexing_Table.xlsx	Complete alternate functions, default carrier usage and count checks
RK3588 Datasheet	Reference for processor, graphics, multimedia and interface capabilities
Compatible Carrier Hardware Documentation	Verify mounting, interface integration and default peripheral scope

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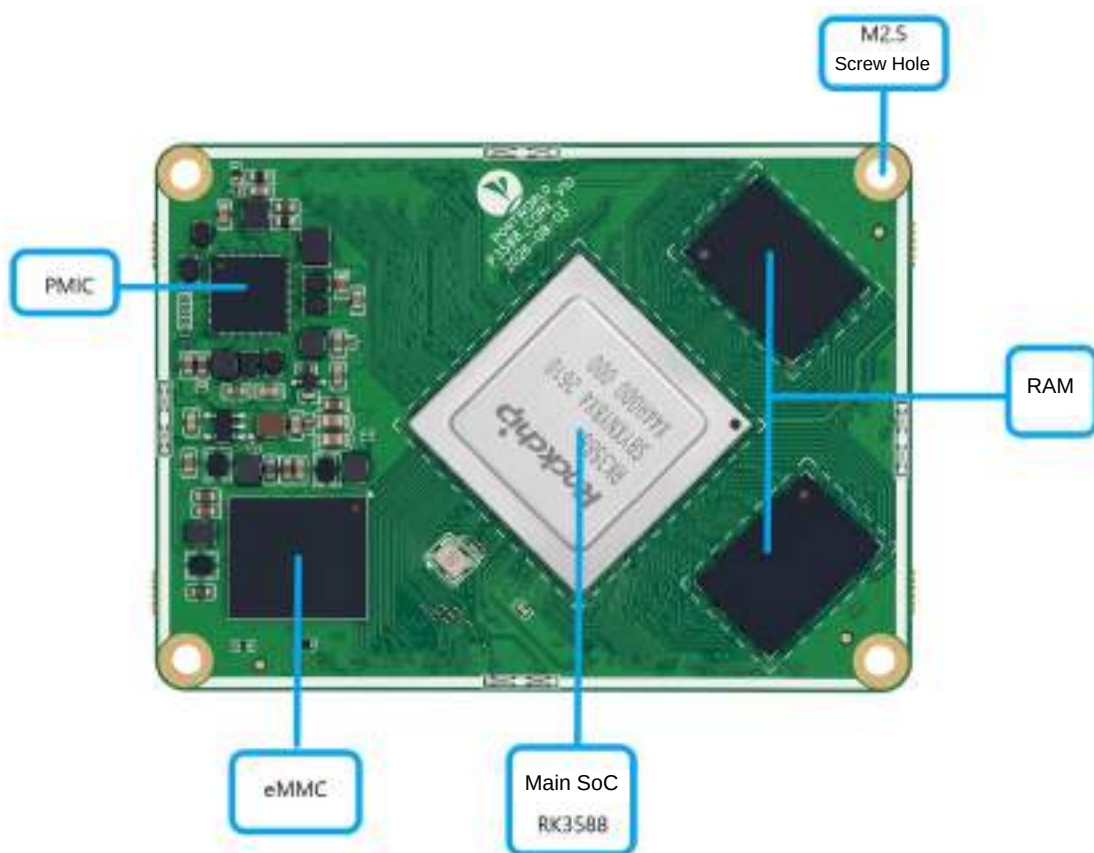
Chapter 1 P3588_CORE_V10 Product Overview

P3588_CORE_V10 is a Rockchip RK3588 core module with four 100-pin board-to-board connectors, designed for edge computing, multimedia terminals, industrial control and embedded devices. The four connectors provide display, camera, USB, PCIe, Ethernet, serial, audio, storage-control and power-management interfaces to the carrier.

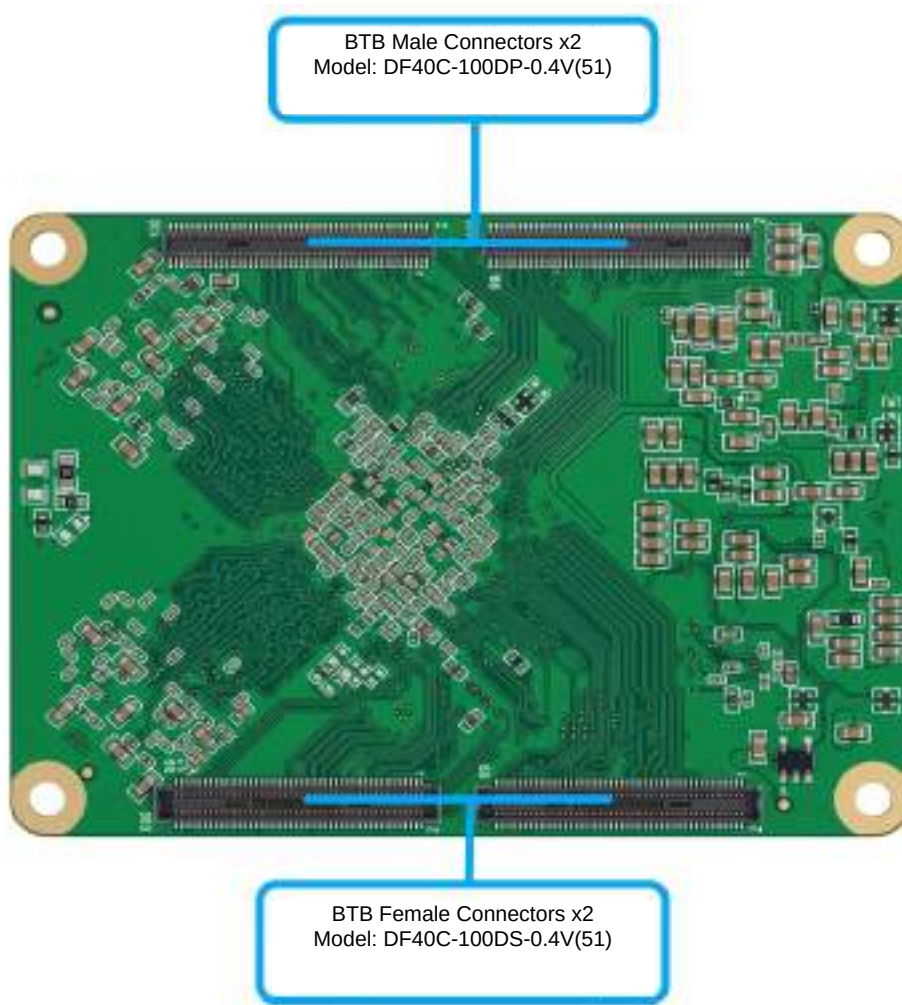
P3588_CORE_V10 shares the schematics, netlist and mechanical definitions of the compatible core module and fits its development carrier. Branding, silkscreen, cover and documentation follow the PORTWORLD P3588_CORE_V10 naming standard.

Core module product photographs:

Front View:



Rear View:



1.1 Product Positioning

- High-compute edge core module supporting 8K video processing and multiple displays.
- Board-to-board connectors suit products requiring flexible interface expansion and custom carriers.
- Compatible mechanical, electrical and interface definitions can shorten system validation cycles.
- Suitable for designs meeting the ambient-temperature and power requirements in this specification.

1.2 Naming and Versions

Item	Details
Product Name	P3588_CORE_V10
Board Silkscreen	PORTWORLD P3588_CORE_V10 2026-08-03
Document Version	V1.1
Release Date	2026-09-10
Compatible Carrier Board	YC Development Carrier Board

Item	Details
Compatibility	Mechanical dimensions, connector definitions, pin nets, key electrical structure and system support remain consistent

1.3 Compatibility Limits

This specification covers the P3588_CORE_V10 core module itself. The carrier is a separate hardware product; its components, interface expansion, connector lifetime and external-device compatibility must also comply with its own documentation. Combined-system functions and actual performance additionally depend on the image, device tree, peripheral load and cooling conditions.

1.4 Board Versions

Board	Version / Silkscreen	Changes
P3588_CORE_V10 Core Module	PORTWORLD P3588_CORE_V10 2026-08-03	Initial version; interfaces and pin definitions match the compatible platform
Compatible Development Carrier	YC	Initial compatible carrier version

Chapter 2 RK3588 Overview

Rockchip RK3588 is a high-performance, low-power processor for ARM computers, edge-computing devices, multimedia terminals and embedded controllers. P3588_CORE_V10 uses RK3588 as its main processor; module circuitry provides RAM, eMMC, power management and board-to-board interfaces.

2.1 Core Configuration

Item	Specification
CPU	Quad-core Cortex-A76 + quad-core Cortex-A55
GPU	Arm Mali-G610 MP4
NPU	Up to 6 TOPS; mixed INT4, INT8, INT16 and FP16 inference
PMIC	RK806-1
Auxiliary Power Controllers	RK860-2、RK860-3
Memory	4GB, 8GB or 16GB options/customization; actual capacity per BOM
Storage	eMMC 32GB, 64GB or 128GB options; actual capacity per BOM
Connectors	Four 100-pin board-to-board connectors; see J1-J4
Dimensions	52mm x 72mm
Operating Systems	Ubuntu 20.04、Ubuntu 22.04、Debian 11、Android 12, Android 13, Android 14, etc.

2.2 Main Functional Blocks

Module	Main Capabilities
Processor	8-core CPU with big/little-core scheduling and multimedia processing
Graphics	Mali-G610 MP4; OpenGL ES 1.1/2.0/3.2, OpenCL 2.2 and Vulkan 1.2
AI Acceleration	NPU up to 6 TOPS; model conversion from TensorFlow, MXNet, PyTorch, Caffe, etc.
Display	HDMI, eDP, DP, MIPI-DSI and independent multi-display output
Video	H.265, H.264, AV1, VP9 and AVS2 decoding; H.264/H.265 encoding

Module	Main Capabilities
Camera	Multiple MIPI-CSI inputs with DPHY/CPHY multiplexing
Network	Dual GMAC; 10/100/1000Mbps Ethernet PHY interfaces
Expansion Interfaces	PCIe, USB, SATA, SD/MMC, UART, SPI, I2C, PWM, CAN and ADC
Audio	I2S/PCM audio buses; headphone, microphone and speaker control signals

2.3 RK3588 Processor Illustration:

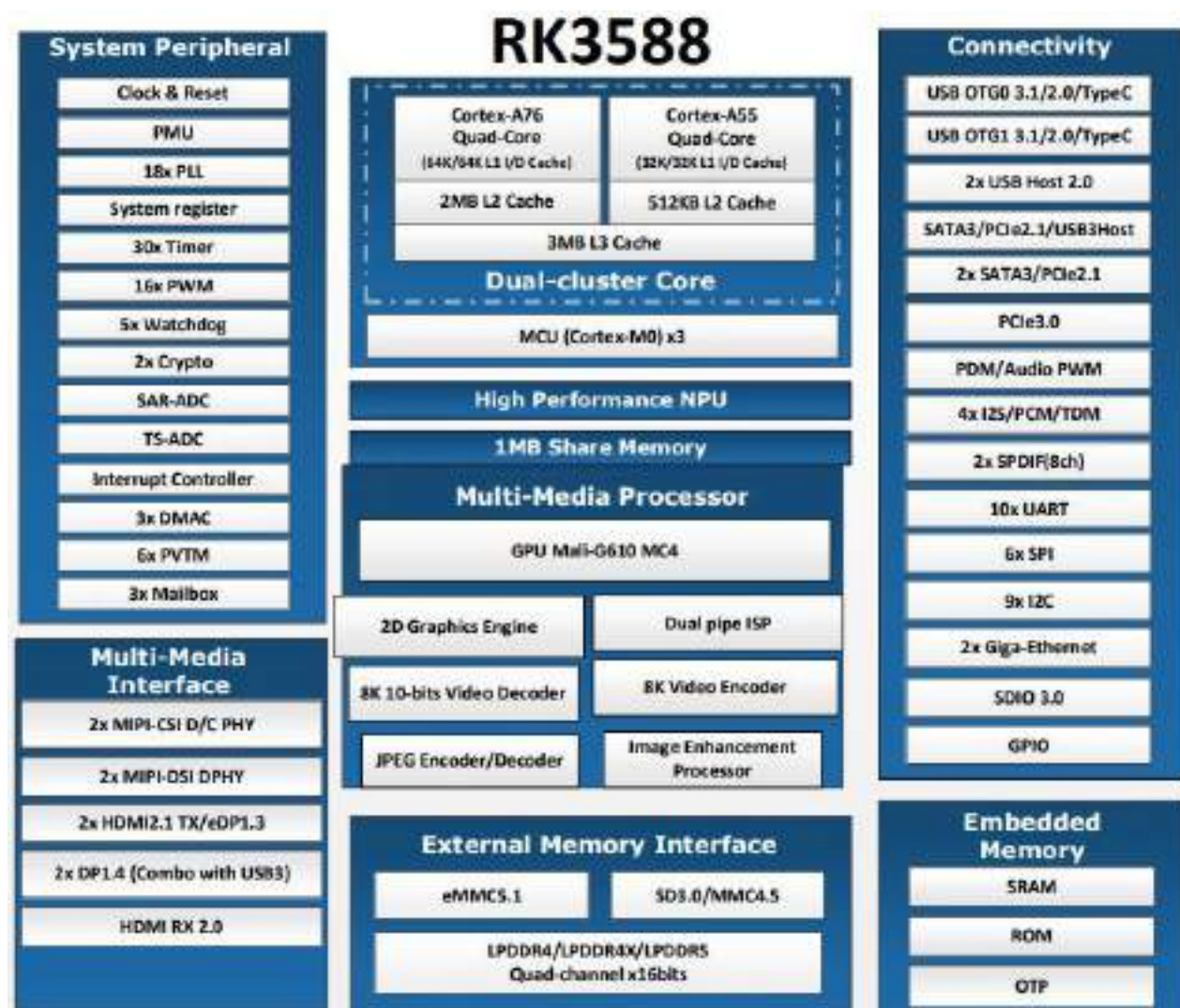


Figure 2-1 P3588_CORE_V10 Core Module Product Image

Chapter 3 Performance and Electrical Specifications

3.1 Processor Clock Frequencies

Item	Minimum	Typical / Options	Maximum	Unit
Cortex-A55 Clock	408	600、816、1008、1200、1416、1608	1800	MHz
Cortex-A76 Clock	408	600、816、1008、1200、1416、1608、1800、2016、2208	2304	MHz
Mali-G610 Clock	300	400、500、600、700、800、900	1000	MHz

3.2 Multimedia Capabilities

Category	Specification
Video Decoding	H.265/VP9 up to 8K@60fps; H.264 up to 8K@30fps; AV1 up to 4K@60fps
Video Encoding	H.264/H.265 up to 8K@30fps
Image Processing	48MP ISP; HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehazing and fisheye correction
Display Output	HDMI 2.1, eDP, DP and MIPI-DSI; independent multi-display output, up to 8K@60Hz
Display Input	HDMI 2.0 RX for video capture and display input

3.3 Power Parameters

Name	Specification				Notes
	Min.	Typ.	Max.	Unit	
Main Supply Voltage	11.5	12	12.5	V	Carrier: 12V@2A or higher recommended Excludes high-power external peripherals
Main Supply Current	-	0.5	-	A	
3S Li-ion Battery Voltage	10.5	12	12.6	V	Compatible carrier supports 3S batteries
Core Module Input Voltage	4.0	5.0	5.5	V	Output net: VCC4V0_SYS; actual rails per schematics and BOM Recommended module supply capacity: 5V@2A
Core Module Current	-	1.0	-	A	

Note: VCC4V0_SYS net naming and the system power tree must follow P3588_CORE_V10 schematics. Carrier input, module input and internal rails have different voltage levels and must be labeled separately during design and testing.

3.4 Environmental Conditions

Item	Environment	Min.	Typ.	Max.	Unit
Temperature	Operating	0	25	60	°C
	Storage	-40	25	+125	°C
Humidity	Operating	10	-	80	%RH
	Storage	5	-	95	%RH

3.5 Interface Speeds

Interface	Maximum Rate	Notes
UART	4Mbps	Asynchronous serial; multiple alternate functions
USB 3.0	5Gbps	USB 2.0 compatible
USB 2.0	480Mbps	High-speed mode
SPI	50MHz	Configurable master/slave modes
I2C	400Kbps	100Kbps typical
PCIe 2.0 x1	5Gbps	Reference maximum throughput: approx. 500MB/s
PCIe 3.0 x1	8GT/s	Backward compatible with PCIe 2.0/1.1
eDP	5.4Gbps/lane	Multiplexed with HDMI 2.1 TX
MIPI DPHY	2.5Gbps/lane	DSI, CSI and DPHY/CPHY multiplexing
SATA 3.0	6Gbps	Supports 1.5Gbps, 3Gbps and 6Gbps

Chapter 4 Mechanical Design and Structure

4.1 Overall Dimensions

Item	Specification
Core Module Size	52mm x 72mm
Connector Count	4 sets
Pins per Connector	100Pin
Total Pins	400Pin
Mechanical Compatibility	Mounting compatible with corresponding module and carrier
Assembly Requirements	Align fully and press vertically; avoid one-sided force

4.2 Connector Definitions

Connectors	Pin Count	Mating Connector Model	Purpose
J1-J4	100 pins/set	DF40C-100DP-0.4V(51)	Module-side male connector
Corresponding Carrier Connector	100 pins/set	DF40C-100DS-0.4V(51)	Carrier-side female connector

Connector location, orientation, Pin 1 marking and height match the compatible module. Verify male/female orientation, Pin 1 position and board spacing; never force connectors together before full alignment.

4.3 Carrier Integration

Integration Item	Result	Notes
Overall Dimensions	Fully compatible	Identical core module dimensions
Connector Location	Fully compatible	Identical J1-J4 positions and orientations
Pinout	Fully compatible	Identical 400-pin nets and default functions
Signal Levels	Same-platform definitions	Use 3.3V, 1.8V and dedicated pins according to the multiplexing table
System Support	platform	Supports the same system families
System Performance	Depends on complete-system conditions	Validate power, temperature rise and peripheral capability under actual system conditions

Chapter 5 Interface Resources

5.1 High-Speed Interfaces

Interface	Quantity	Main Specifications
USB 3.0 HOST/OTG	1	Comprises USB 2.0 OTG and USB 3.0 SuperSpeed lanes; up to 5Gbps
USB 2.0 HOST	2	Two independent USB 2.0 HOST interfaces
USB 2.0 HOST/OTG	1	Supports ID and VBUS detection
PCIe 2.x	1	Up to 5Gbps; peripherals or multiplexing with SATA and other functions
PCIe 3.x	Up to 2 groups	Up to 8GT/s/lane; x1/x2/x4 combinations
SATA 3.0	Up to 3	eSATA compatible; 1.5/3/6Gbps
SD/MMC HOST	1	Includes CLK, CMD, D0-D3 and DET

5.2 Display and Camera

Interface	Quantity	Main Specifications
HDMI TX	2	HDMI 2.1; total bandwidth up to 24Gbps; 8K@60Hz output
HDMI RX	1	HDMI 2.0 input, up to 4K@60fps
MIPI-DSI	Up to 2	Up to 4 data lanes per port; each lane up to 2.5Gbps
MIPI-CSI	Up to 6	4-lane DPHY or two 2-lane groups; DPHY/CPHY multiplexing
eDP	1	Multiplexed with HDMI TX; up to 5.4Gbps/lane

5.3 General-Purpose, Network and Audio Interfaces

Interface	Available Count	Notes
Ethernet	2	Dual GMAC; RGMII connection to 10/100/1000Mbps PHY
UART	Up to 8	Includes UART2 debug port and RS232/RS485 multiplexed serial ports
SPI	Up to 5	Two chip selects per controller

Interface	Available Count	Notes
FSPI	1	For SPI Flash connection
PWM	Up to 15	For backlight, fan, power-enable and peripheral control
ADC	7	Routed through BTB; input range 0-1.8V
I2S/PCM	1	I2S0 supports 8-channel TX and 8-channel RX
I2C	Up to 8	I2C0 controls the module's internal RK860
CAN	2	CAN1_M1 and CAN2_M0 recommended; external transceivers required
Audio	1	Headphone, microphone and speaker control signals

Chapter 6 Pin Definitions and Multiplexing

6.1 Connector Statistics

Connectors	Pin Count	Alternate Function Entries	Default Carrier Usage
J1	100	269	63
J2	100	308	77
J3	100	253	77
J4	100	283	70
Total	400	1113	287

6.2 Pin Marking Guide

Marking	Meaning
[1]	Dedicated pin; cannot be used as general GPIO
[2]	CPU boot-related pin; general I/O use not recommended
[3]	Unused by default on companion carrier
Default Function	Recommended P3588_CORE_V10 device-tree configuration
Default Carrier Usage	Alternate function used by the carrier's default configuration

6.3 Pin Category Statistics

Category	Physical Pin Count
GPIO	124
Ground	86
MIPI	60
Display	48
PCIe	26
Power / Control	20
USB	16
SATA	8

Category	Physical Pin Count
ADC	6
Unused	4
Other	2

6.4 Companion Multiplexing Table

P3588_CORE_V10_Pin_Multiplexing_Table.xlsx lists all 400 pins and 1113 alternate-function entries, including the pin overview, alternate-function details, original matrix, color legend and automatic checks. Pin data matches the compatible baseline cell by cell; differences: 0.

- Pin overview: one physical pin per row; nets, categories, levels, default carrier usage and alternate-function counts.
- Alternate-function details: one function per row, 1113 entries total; filter by interface or function.
- Original matrix: preserves J1-J4 left/right sides and original alternate-function column positions.
- Legend and validation: color meanings, quantity statistics and automatic validation status.

Chapter 7 Power and Hardware Design

7.1 Power Input

The module receives power from the carrier via VCC4V0_SYS. Carrier step-down and power management supply the appropriate rails to the module, DDR, processor and peripherals. PMIC: RK806-1; auxiliary controllers: RK860-2 and RK860-3.

Level	Specification	Design Notes
Carrier DC Input	12V; 2A or higher recommended	Must support peak board and peripheral loads
Core Module Input	4.0-5.5V	Input net: VCC4V0_SYS
PMIC	RK806-1	Module Main Power Management
Auxiliary Power Control	RK860-2、RK860-3	Controls core and peripheral power rails
Protection and Filtering	Follow schematics	Power input must meet ripple, surge and power-on sequencing requirements

7.2 Boot, Reset and Power Control

Signal	Function	Design Recommendations
AUTO_PWRON_EN	Automatic Power-On Enable	Configure per carrier and image requirements
PWR_ON	Power On/Off Control	Add necessary filtering and ESD protection when connecting buttons or control circuits
RESETn	System Reset Input	Active low; hold time must meet RK3588 reset requirements
EXT_PWR_EN	Peripheral Power Enable	Controls carrier power domains; do not exceed pin drive capability
SARADC_IN0_BOOT	MaskROM Mode Detection	For flashing and recovery; avoid general ADC use
SARADC_IN1/Recovery	Recovery Mode Detection	For system recovery and image flashing

7.3 Hardware Design Precautions

- Power distribution: connect every power and GND pin as defined; never carry the whole board's current through one pin.
- Signal levels: use 3.3V, 1.8V and dedicated pins per the multiplexing table; external devices must remain within their voltage domains.
- Differential signals: maintain continuous reference planes and controlled impedance for HDMI, PCIe, USB SuperSpeed, MIPI, SATA and Ethernet differential pairs.
- Reset and boot: RESETn, PWR_ON, RECOVERY and MASKROM circuits must ensure reliable sequencing and button operation.

- Cooling: test temperature rise under high load for the actual ambient temperature and mounting space; add a heatsink or airflow if needed.
- ESD and surge: add ESD, surge and overcurrent protection to external interfaces for the application environment.
- Connector assembly: verify orientation, Pin 1 and board spacing; avoid angled insertion and one-sided force.

Chapter 8 Compatible Carrier Hardware Specifications

P3588_CORE_V10 fits the compatible development carrier, which provides DC input, standard connectors, buttons, indicators and expansion connections. The following specifications describe combined-system capabilities. Carrier appearance, components and trademarks remain subject to the original manufacturer's documentation.

8.1 Carrier Hardware Specifications

Function	Specification
Power	12V@2A or higher DC input; one DC input and one power output connector
HDMI 2.0 Input	One vertical standard HDMI input; up to 4K@60fps
HDMI 2.1 Output	Two vertical standard HDMI outputs; up to 8K@60Hz
MIPI-DSI	Two display connectors; 30-pin 0.5mm FPC and 4-lane output
MIPI-CSI	Six 24-pin FPC camera connectors for corresponding MIPI modules
Ethernet	Two Gigabit Ethernet ports; 10/100/1000Mbps auto-negotiation
USB	One USB 3.0 Type-A OTG; three USB 2.0 Type-A HOST; one DP1.4/USB 3.0 Type-C OTG
PCIe x4 Slot	PCIe 3.0 x2 lane for PCIe expansion devices
Mini PCIe	PCIe 2.0 x1 for WLAN, 4G/5G or multiplexed mSATA
M.2 M KEY	PCIe 3.0 x2 lane; supports 2280 M.2 SSD
M.2 E KEY	PCIe 2.0 x1; supports M.2 A+E WLAN cards
SATA	One standard SATA data connector and one SATA power connector; 12V output
SIM Card	One NanoSIM socket; requires Mini PCIe 4G/5G module
Audio	One 3.5mm headphone/microphone combo jack; one MIC and two SPK connectors
Serial Ports	One debug port, default 1500000-8-N-1; two RS232 and two RS485 ports
CAN	Two CAN buses; up to 1Mbps
ADC	Three ADC acquisition interfaces; input 0-1.8V
FAN	One 2-pin 1.5mm fan connector; 5V/12V fans
RTC	One 2-pin 1.25mm RTC battery connector
SPI Flash	Reserved SPI Flash pads; unpopulated by default
Infrared	One onboard infrared remote-control receiver

Function	Specification
TF Card	MicroSD/TF boot and storage; up to 512GB
Buttons	One each: PWR, RESET, RECOVERY and MASKROM
Dimensions	173mm x 96mm

8.2 Carrier Interface Resources

Interface	Quantity	Main Parameters
HDMI 2.1 Output	2	Standard HDMI socket; up to 8K@60Hz; steady power approx. 2.5W, hot-plug peak approx. 4.6W
Ethernet	2	RJ45 with RTL8211F; supports 10/100/1000Mbps; cable connected, no load: approx. 2W
USB 3.0 HOST	1	Type-A; USB 3.1 Gen1, up to 5Gbps; maximum output current 2000mA
USB 2.0 HOST	3	Type-A; 480Mbps, 12Mbps and 1.5Mbps; shared supply maximum 2000mA
DP1.4/USB 3.0 OTG	1	Type-C; firmware flashing, OTG debugging and DP1.4 output, up to 4K@60Hz
Mini PCIe	1	PCIe 2.0 x1, up to 5GT/s; multiplexed mSATA; maximum continuous output 2.5A
M.2	2	M.2 E KEY: PCIe 2.0 x1; M.2 M KEY: PCIe 3.0 x2; supports 2280 SSD
SATA	1	Standard SATA data and power connectors; supports 2.5- or 3.5-inch drives
WiFi/BT	Up to 1	Expansion via Mini PCIe or M.2 E KEY
4G/5G	Up to 1	Expansion via Mini PCIe; requires SIM card
MIPI-DSI	2	30-pin 0.5mm FPC, 4-lane; per display up to 1920x1080@60fps
MIPI-CSI	6	24-pin FPC camera connector; matching adapter cable required
Debug Serial Port	1	1x3P 2.54mm header; default 1500000-8-N-1
UART	2	PH-4A 1x4P, 2mm pitch; shared with RS232/RS485 via jumpers
RS232	2	WJ15EDGRC-3.81-6P via SIT3232 transceivers
RS485	2	WJ15EDGRC-3.81-4P via SIT3088 transceivers
CAN	2	WJ15EDGRC-3.81-4P via CAN transceivers; up to 1Mbps

Interface	Quantity	Main Parameters
ADC	3	PH-6A, 2mm pitch; input 0-1.8V
Audio	1	3.5mm headphone input/output combo jack
Microphone	1	PH2.0 2P; shares headphone microphone input signal
Speaker	1	PH2.0 2P; output power approx. 1W
Power Output	1	PH-6A; supports 3.3V@2A, 5V@2A and 12V@1A

Mini PCIe uses PCIe for WiFi cards, USB for 4G/5G modules and SATA when multiplexed as mSATA. The protocol depends on the installed module and carrier configuration.

Chapter 9 Compatible Carrier Operating Instructions

9.1 Power Input

Use a 12V@2A or higher DC supply. The carrier converts 12V to the voltages required by the module and peripherals.

The module supply DC-DC enables only above 7.7V input. A steady red power indicator shows normal input power.

Item	requirements
DC Connector	DC-044A-20A; accepts DC5.5x2.1 and DC5.5x2.5 plugs
Overload Protection	Downstream resettable fuse; trip current approx. 4A
Input Voltage Limit	Do not exceed 18V; DC-DC and downstream devices may be damaged
SATA Power	Use 12V when connecting SATA drives to avoid insufficient power or voltage mismatch
Power Output	PH-6A 6-pin output supports 3.3V, 5V and 12V; increase main supply power for external loads

9.2 Buttons and Boot

Buttons	Function	Related Signal
ON/OFF	System on/off or sleep control	PWR_ON
RESET	System reset	RESETn
RECOVERY	Enter Recovery mode for image flashing	SARADC_IN1/Recovery
MASKROM	Enter MaskROM mode for image flashing	SARADC_IN0_BOOT

9.3 eMMC Flashing

- MaskROM: with power disconnected, connect Type-C OTG and hold MASKROM. Apply power; release the button after the flashing tool detects the device.
- Recovery: with power disconnected, connect Type-C OTG and hold RECOVERY. Apply power; release the button after the tool detects the LOADER device.
- If Android image download fails, erase Flash, then power up again in MaskROM mode and flash.

9.4 Indicators, TF Card and SIM Card

- PWR illuminates when module power is normal and turns off at shutdown or power removal.
- SYS is controlled by GPIO1_C6 and can be configured for heartbeat blinking after normal boot.
- MicroSD/TF supports boot and storage up to 512GB. Do not remove or insert the boot card while the system is running.

- Use a NanoSIM with a Mini PCIe 4G/5G module.

9.5 Network, USB, Display and Audio

Two Gigabit ports use RTL8211F-series PHYs. USB3.0 OTG connects to Type-C for flashing, OTG debugging and DP output; another USB3.0 controller connects to Type-A USB3.0. USB2.0 HOST is expanded by a HUB to multiple USB-A ports and expansion-module connections.

Video outputs comprise two HDMI 2.1 ports and two MIPI-DSI display interfaces. The ES8388 codec provides headphone, microphone and speaker functions; speaker output is approx. 1W. Supported resolutions, sample rates and hot-plug capability depend on the carrier and software configuration.

9.6 Expansion Interfaces

Interface	Operating Notes
Mini PCIe	Supports WiFi, 4G/5G and mSATA; verify module protocol and power requirements before installation
M.2 E KEY	Supports M.2 A+E WLAN; verify module definitions when using PCIe or USB lanes
M.2 M KEY	Supports 2280 NVMe SSD over PCIe 3.0 x2
SATA	Standard SATA data/power connectors; ensure adequate 12V power for drives
FAN	2-pin 1.5mm fan connector; PWM speed control; verify polarity
RTC	2-pin 1.25mm connector for external RTC battery
Debug UART	1x3P 2.54mm header, default 1500000-8-N-1; boot logs and system debugging
IR	Onboard IR receiver for remote reception and system control

9.7 Serial Ports, CAN and SARADC

Two UARTs switch between RS232 and RS485 via jumpers. Both RS232 channels share one connector; both RS485 channels share one connector. CAN supports CAN1_M1 and CAN2_M0; fit 120-ohm bus termination. SARADC accepts 0-1.8V for external buttons or potentiometer sampling.

- RS232 uses SIT3232-series transceivers; maximum communication settings depend on carrier and software configuration.
- RS485 uses SIT3088-series transceivers; select UART signals using jumpers.
- Use standard CAN transceivers, correct wiring and termination resistors.
- SARADC input must not exceed 1.8V; current limiting and ESD protection are recommended.

Chapter 10 Reference Power Consumption

These reference tests use the same hardware platform as P3588_CORE_V10 and a compatible carrier. Results depend on image version, peripherals, cooling, storage and ambient temperature; they do not guarantee system power consumption or temperature rise. P3588 systems must use actual test reports obtained with matching images and peripheral conditions.

10.1 Test Methods

Test Item	Test Procedure
Boot / Idle	Restart three times and record the peak; idle for 20 minutes after boot to record stable current, power and SoC temperature
Sleep	Use freeze or power-button sleep; record steady values
Full Load	Run s-tui and stress at full CPU load for 20 minutes; record peak, average and temperature
Android Stress Test	Run AnTuTu v10.3.7 stress test for 45 minutes

10.2 Complete-Board Linux Reference Power

System / Type	Test Procedure	Peak Current / mA	Steady Current / mA	Peak Power / mW	Steady Power / mW	SoC Temp. / deg C
Ubuntu20.04 lite	Boot / Idle	1000.5	420.9	12141.9	5171.6	45.3
Ubuntu20.04 lite	Sleep	-	309.7	-	3816	-
Ubuntu20.04 lite	Full Load	861.8	733.3	10493.1	8941.8	40.7/84.1
Ubuntu20.04 gnome	Boot / Idle	1013.9	418.7	12298.1	5146.8	41.6
Ubuntu20.04 gnome	Sleep	-	306.3	-	3775.2	-
Ubuntu20.04 gnome	Full Load	869.8	715.1	10534.1	8685.4	42.5/84.1
Ubuntu22.04 desktop	Boot / Idle	1082.4	412	13045	5053.8	43.5
Ubuntu22.04 desktop	Sleep	-	290.5	-	3578	-
Ubuntu22.04 desktop	Full Load	915.3	734.1	11042.8	8904.6	47.2/85
Ubuntu22.04 server	Boot / Idle	1025.8	422.6	12412.8	5187	43.5
Ubuntu22.04 server	Sleep	-	307.8	-	3794.2	-
Ubuntu22.04 server	Full Load	892.3	735.2	10835.7	8951.9	43.5/85

System / Type	Test Procedure	Peak Current / mA	Steady Current / mA	Peak Power / mW	Steady Power / mW	SoC Temp. / deg C
Debian11 lite	Boot / Idle	1004	554.2	12204.5	6799.8	42.5
Debian11 lite	Sleep	-	347.7	-	4284.6	-
Debian11 lite	Full Load	833.6	703.5	10180.5	8602.2	43.5/84.1
Debian11 gnome	Boot / Idle	1041.6	440.9	12517.9	5395	42.5
Debian11 gnome	Sleep	-	344.7	-	4230	-
Debian11 gnome	Full Load	844.8	693.6	10280.9	8465.7	59.2/84.1

10.3 Complete-Board Android Reference Power

Display Configuration	Test Procedure	Peak Current / mA	Steady Current / mA	Peak Power / mW	Steady Power / mW
HDMI	Boot / Idle	976.3	437.5	11870.3	5380.1
HDMI	Sleep	-	453.9	-	5556.2
HDMI	AnTuTu Benchmark	1170.9	718.7	14013.7	8702.9
MIPI 10.1-inch 800p	Boot / Idle	1098.8	489.5	13240.3	5986.6
MIPI 10.1-inch 800p	Sleep	-	289.2	-	3559.3
MIPI 10.1-inch 800p	AnTuTu Benchmark	1224.4	790.5	14699	9591.9
MIPI 5.5-inch 1080p	Boot / Idle	1079.2	454.4	13075.1	5580.3
MIPI 5.5-inch 1080p	Sleep	-	282	-	3479.2
MIPI 5.5-inch 1080p	AnTuTu Benchmark	1193.5	738.1	14459	8998.9

10.4 Standalone Module Idle Reference Power

System	Image Type	Test Procedure	Peak Current / mA	Steady Current / mA	Peak Power / mW	Steady Power / mW
Android12	HDMI	Idle	408.1	403.4	2118.9	2094.6
Debian11	lite	Idle	347.7	327.4	1809	1703.5
Ubuntu20.04	lite	Idle	460.7	454.9	2390	2360.1
Ubuntu22.04	desktop	Idle	261.2	259.1	1360.4	1349.8

Chapter 11 Software Support

System	Series	Notes
Ubuntu	20.04, 22.04	Linux desktop or server images
Debian	11	Lightweight or server images
Android	12, 13, 14	Multimedia and display applications

Software support matches the compatible module. Released images, kernel versions, U-Boot and device-tree configurations are governed by the P3588_CORE_V10 software package. After changing the carrier, peripherals or pin multiplexing, update the device tree and revalidate.

8.1 Software Compatibility Limits

- The factory device tree supports only the defined core-module connectors and companion-carrier peripheral combinations.
- Custom carriers with different power enables, reset, display or expansion interfaces require device-tree reconfiguration.
- Storage capacity, display outputs and network settings for Android/Linux images are governed by their release packages.

Chapter 12 Compatible Carrier Notes

P3588_CORE_V10 fully fits the compatible development carrier. Mechanical dimensions, connector positions, 400-pin nets, default functions, power structure and system support remain consistent.

Check Item	Result	Notes
Mechanical Mounting	Compatible	All module connectors align fully
Pinout	Compatible	Identical J1-J4 pin nets
Alternate Functions	Compatible	1113 alternate-function entries match the baseline
Default Carrier Peripherals	Compatible	287 alternate functions marked for default carrier usage
Operating Systems	Compatible	Supports the same system families
Complete System Performance	Validate complete system	Power, temperature rise, interface speeds and peripheral compatibility depend on actual configuration

Carrier and expansion-module names and trademarks belong to their respective owners. This specification describes hardware compatibility only; it does not replace the carrier's technical manual, warranty terms or documentation licenses.

Chapter 13 Ordering and Version Control

10.1 Model Information

Item	Specification
Product Model	P3588_CORE_V10
Board Silkscreen	PORTWORLD P3588_CORE_V10 2026-08-03
Document Version	V1.1
Memory Options	4GB, 8GB, 16GB or custom configurations
Storage Options	32GB, 64GB, 128GB or custom configurations
Carrier Pairing	Compatible carrier

10.2 Version Maintenance

- When silkscreen revisions change, update the specification, BOM, assembly documents and test records.
- After changes to RAM, eMMC, PMIC, connectors or other key parts, recheck pin definitions, power and system compatibility.
- After image, kernel, U-Boot or device-tree upgrades, revalidate boot, display, networking and storage.
- After pin-multiplexing or default carrier usage changes, update the companion Excel file and difference-validation report.

10.3 Data Limits

This document lists specifications and compatibility directly related to module hardware design. Power, temperature rise, EMC, ESD, long-term reliability, storage life and extreme-environment performance require separate P3588_CORE_V10 test reports or certification documents.

Pin data is governed by the P3588_CORE_V10 netlist and companion multiplexing table. If schematics, netlist, BOM, device tree or carrier revision changes, the latest controlled files supersede the corresponding data here.

Appendix A J1 Pin Summary

J1 has 100 pins. The table lists net names, categories, voltage/properties, default carrier usage and alternate-function counts. See the companion Excel file for complete function names.

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
1	VCC4V0_SYS(input)	Power / Control	4V Power Input	No	1	VCC4V0_SYS(input)
2	VCC4V0_SYS(input)	Power / Control	4V Power Input	No	1	VCC4V0_SYS(input)
3	VCC4V0_SYS(input)	Power / Control	4V Power Input	No	1	VCC4V0_SYS(input)
4	VCC4V0_SYS(input)	Power / Control	4V Power Input	No	1	VCC4V0_SYS(input)
5	VCC4V0_SYS(input)	Power / Control	4V Power Input	No	1	VCC4V0_SYS(input)
6	VCC4V0_SYS(input)	Power / Control	4V Power Input	No	1	VCC4V0_SYS(input)
7	GND	Ground	GND	No	1	GND
8	GND	Ground	GND	No	1	GND
9	GND	Ground	GND	No	1	GND
10	GND	Ground	GND	No	1	GND
11	GND	Ground	GND	No	1	GND
12	GND	Ground	GND	No	1	GND
13	VCC_3V3_S3(output)	Power / Control	3.3V	No	1	VCC_3V3_S3(output)
14	VCC_3V3_S3(output)	Power / Control	3.3V	No	1	VCC_3V3_S3(output)
15	VCCA_3V3_S0(output)	Power / Control	3.3V	No	1	VCCA_3V3_S0(output)
16	VCCA_3V3_S0(output)	Power / Control	3.3V	No	1	VCCA_3V3_S0(output)
17	VCCA_1V8_S0(output)	Power / Control	1.8V	No	1	VCCA_1V8_S0(output)

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
18	VCCA_1V8_S0(output)	Power / Control	1.8V	No	1	VCCA_1V8_S0(output)
19	VCC_1V8_S3(output)	Power / Control	1.8V	No	1	VCC_1V8_S3(output)
20	VCC_1V8_S3(output)	Power / Control	1.8V	No	1	VCC_1V8_S3(output)
21	VCC_1V8_S0(output)	Power / Control	1.8V	No	1	VCC_1V8_S0(output)
22	VCC_1V8_S0(output)	Power / Control	1.8V	No	1	VCC_1V8_S0(output)
23	GND	Ground	GND	No	1	GND
24	AUTO_PWRON_EN	Power / Control	Dedicated	Yes	1	AUTO_PWRON_EN
25	MIPI_CSI1_CLK1P	MIPI	Dedicated	Yes	1	MIPI_CSI1_CLK1P
26	RESETn	Power / Control	Dedicated	Yes	1	RESETn
27	MIPI_CSI1_CLK1P	MIPI	Dedicated	Yes	1	MIPI_CSI1_CLK1P
28	PWR_ON	Power / Control	Dedicated	Yes	1	PWR_ON
29	GND	Ground	GND	No	1	GND
30	EXT_PWR_EN	Power / Control	Dedicated	No	1	EXT_PWR_EN
31	MIPI_CSI1_D3P	MIPI	Dedicated	Yes	1	MIPI_CSI1_D3P
32	GND	Ground	GND	No	1	GND
33	MIPI_CSI1_D3N	MIPI	Dedicated	Yes	1	MIPI_CSI1_D3N
34	MIPI_CSI0_CLK1P	MIPI	Dedicated	Yes	1	MIPI_CSI0_CLK1P
35	MIPI_CSI1_D2P	MIPI	Dedicated	Yes	1	MIPI_CSI1_D2P
36	MIPI_CSI0_CLK1N	MIPI	Dedicated	Yes	1	MIPI_CSI0_CLK1N
37	MIPI_CSI1_D2N	MIPI	Dedicated	Yes	1	MIPI_CSI1_D2N

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
38	GND	Ground	GND	No	1	GND
39	MIPI_CSI1_CLK0P	MIPI	Dedicated	Yes	1	MIPI_CSI1_CLK0P
40	MIPI_CSI0_D3P	MIPI	Dedicated	Yes	1	MIPI_CSI0_D3P
41	MIPI_CSI1_CLK0N	MIPI	Dedicated	Yes	1	MIPI_CSI1_CLK0N
42	MIPI_CSI0_D3N	MIPI	Dedicated	Yes	1	MIPI_CSI0_D3N
43	MIPI_CSI1_D1P	MIPI	Dedicated	Yes	1	MIPI_CSI1_D1P
44	MIPI_CSI0_D2P	MIPI	Dedicated	Yes	1	MIPI_CSI0_D2P
45	MIPI_CSI1_D1N	MIPI	Dedicated	Yes	1	MIPI_CSI1_D1N
46	MIPI_CSI0_D2N	MIPI	Dedicated	Yes	1	MIPI_CSI0_D2N
47	MIPI_CSI1_D0P	MIPI	Dedicated	Yes	1	MIPI_CSI1_D0P
48	GND	Ground	GND	No	1	GND
49	MIPI_CSI1_D0N	MIPI	Dedicated	Yes	1	MIPI_CSI1_D0N
50	MIPI_CSI0_CLK0P	MIPI	Dedicated	Yes	1	MIPI_CSI0_CLK0P
51	GND	Ground	GND	No	1	GND
52	MIPI_CSI0_CLK0N	MIPI	Dedicated	Yes	1	MIPI_CSI0_CLK0N
53	GPIO4_C6	GPIO	1.8V	Yes	6	GPIO4_C6 / GMAC0_TXER / PWM7_IR_M3 / SPI3_CLK_M0 / UART7_CTSN_M0
54	GND	Ground	GND	No	1	GND
55	GPIO2_C5	GPIO	1.8V	Yes	2	GPIO2_C5 / CLK32K_OUT1
56	MIPI_CSI0_D1P	MIPI	Dedicated	Yes	1	MIPI_CSI0_D1P

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
57	GPIO2_C3	GPIO	1.8V	Yes	5	GPIO2_C3 / ETH0_REFCLK0_25M / I2S2_SDI_M0 / SPI1_CS0_M0 / I2C6_SCL_M2
58	MIPI_CSI0_D1N	MIPI	Dedicated	Yes	1	MIPI_CSI0_D1N
59	GPIO2_C4	GPIO	1.8V	Yes	6	GPIO2_C4 / GMAC0_PPSCCLK / HDMI_TX1_CEC_M0 / SPI1_CS1_M0 / UART9_RX_M0
60	MIPI_CSI0_D0P	MIPI	Dedicated	Yes	1	MIPI_CSI0_D0P
61	GPIO2_B5	GPIO	1.8V	Yes	6	GPIO2_B5 / GMAC0_PPSTRIG / HDMI_TX1_SCL_M0 / FSPI_CS1N_M1 / UART7_TX_M0
62	MIPI_CSI0_D0N	MIPI	Dedicated	Yes	1	MIPI_CSI0_D0N
63	GPIO2_B4	GPIO	1.8V	Yes	6	GPIO2_B4 / GMAC0_PTP_REFCLK / HDMI_TX1_SDA_M0 / FSPI_CS0N_M1 / UART7_RX_M0
64	GND	Ground	GND	No	1	GND
65	GND	Ground	GND	No	1	GND
66	GPIO4_C3	GPIO	1.8V	Yes	6	GPIO4_C3 / GMAC0_MCLKINOUT / I2S2_SDO_M0 / SPI3_CS1_M0 / PWM4_M1
67	GPIO3_B6	GPIO	3.3V	Yes	6	GPIO3_B6 / GMAC1_MCLKINOUT / I2S2_LRCK_M1 /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						UART3_RX_M1 / CAN1_TX_M0
68	GND	Ground	GND	No	1	GND
69	GPIO3_A4	GPIO	3.3V	Yes	7	GPIO3_A4 / GMAC1_TXCLK / SDIO_CMD_M1 / I2S3_SDI / UART8_RTSN_M1
70	GPIO2_C0	GPIO	1.8V	Yes	6	GPIO2_C0 / GMAC0_TXEN / I2S2_LRCK_M0 / SPI1_CLK_M0 / UART1_RTSN_M0
71	GPIO3_B5	GPIO	3.3V	Yes	6	GPIO3_B5 / GMAC1_TXEN / I2S2_SCLK_M1 / UART3_TX_M1 / CAN1_RX_M0
72	GPIO2_B3	GPIO	1.8V	Yes	5	GPIO2_B3 / GMAC0_TXCLK / SDIO_CLK_M0 / FSPI_CLK_M1 / I2C3_SDA_M3
73	GPIO3_B3	GPIO	3.3V	Yes	4	GPIO3_B3 / GMAC1_TXD0 / I2S2_SDO_M1 / UART2_RTSN
74	GPIO2_B6	GPIO	1.8V	Yes	5	GPIO2_B6 / GMAC0_TXD0 / I2S2_MCLK_M0 / UART1_RX_M0 / I2C5_SCL_M4
75	GPIO3_B4	GPIO	3.3V	Yes	4	GPIO3_B4 / GMAC1_TXD1 / I2S2_MCLK_M1 / UART2_CTSN
76	GPIO2_B7	GPIO	1.8V	Yes	5	GPIO2_B7 / GMAC0_TXD1 / I2S2_SCLK_M0 / UART1_TX_M0 / I2C5_SDA_M4
77	GPIO3_A0	GPIO	3.3V	Yes	8	GPIO3_A0 / GMAC1_TXD2 / SDIO_D0_M1 / I2S3_MCLK /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						FSPI_D0_M2
78	GPIO2_B1	GPIO	1.8V	Yes	6	GPIO2_B1 / GMAC0_TXD2 / SDIO_D3_M0 / FSPI_D3_M1 / UART6_CTSN_M0
79	GPIO3_A1	GPIO	3.3V	Yes	9	GPIO3_A1 / GMAC1_TXD3 / SDIO_D1_M1 / I2S3_SCLK / FSPI_D1_M2
80	GPIO2_B2	GPIO	1.8V	Yes	4	GPIO2_B2 / GMAC0_TXD3 / SDIO_CMD_M0 / I2C3_SCL_M3
81	GND	Ground	GND	No	1	GND
82	GND	Ground	GND	No	1	GND
83	GPIO3_B1	GPIO	3.3V	Yes	5	GPIO3_B1 / GMAC1_RXDV_CRS / UART2_TX_M2 / MIPI_CAMERA4_CLK_M1 / PWM2_M1
84	GPIO4_C2	GPIO	1.8V	Yes	5	GPIO4_C2 / GMAC0_RXDV_CRS / PWM2_M2 / SPI3_CS0_M0 / UART7_RTSN_M0
85	GPIO3_A5	GPIO	3.3V	Yes	7	GPIO3_A5 / GMAC1_RXCLK / SDIO_CLK_M1 / FSPI_CLK_M2 / I2C4_SDA_M0
86	GPIO2_B0	GPIO	1.8V	Yes	6	GPIO2_B0 / GMAC0_RXCLK / SDIO_D2_M0 / FSPI_D2_M1 / UART6_RTSN_M0
87	GPIO3_A7	GPIO	3.3V	Yes	4	GPIO3_A7 / GMAC1_RXD0 /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						MIPI_CAMERA2_CLK_M1 / PWM8_M0
88	GPIO2_C2	GPIO	1.8V	Yes	5	GPIO2_C2 / GMAC0_RXD1 / SPI1_MOSI_M0 / UART9_TX_M0 / I2C6_SDA_M2
89	GPIO3_B0	GPIO	3.3V	Yes	4	GPIO3_B0 / GMAC1_RXD1 / MIPI_CAMERA3_CLK_M1 / PWM9_M0
90	GPIO2_C1	GPIO	1.8V	Yes	5	GPIO2_C1 / GMAC0_RXD0 / SPI1_MISO_M0 / UART1_CTSN_M0 / I2C2_SCL_M1
91	GPIO3_A2	GPIO	3.3V	Yes	8	GPIO3_A2 / GMAC1_RXD2 / SDIO_D2_M1 / I2S3_LRCK / FSPI_D2_M2
92	GPIO2_A7	GPIO	1.8V	Yes	5	GPIO2_A7 / GMAC0_RXD3 / SDIO_D1_M0 / FSPI_D1_M1 / UART6_TX_M0
93	GPIO3_A3	GPIO	3.3V	Yes	8	GPIO3_A3 / GMAC1_RXD3 / SDIO_D3_M1 / I2S3_SDO / FSPI_D3_M2
94	GPIO2_A6	GPIO	1.8V	Yes	5	GPIO2_A6 / GMAC0_RXD2 / SDIO_D0_M0 / FSPI_D0_M1 / UART6_RX_M0
95	GPIO3_C2	GPIO	3.3V	Yes	7	GPIO3_C2 / GMAC1_MDC / MIPI_TE0 / SPI1_CS0_M1 / I2C8_SCL_M4
96	GPIO4_C4	GPIO	1.8V	Yes	6	GPIO4_C4 / GMAC0_MDC /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						PWM5_M2 / SPI3_MISO_M0 / UART9_RTSN_M0
97	GPIO3_C3	GPIO	3.3V	Yes	7	GPIO3_C3 / GMAC1_MDIO / MIPI_TE1 / SPI1_CS1_M1 / I2C8_SDA_M4
98	GPIO4_C5	GPIO	1.8V	Yes	6	GPIO4_C5 / GMAC0_MDIO / PWM6_M2 / SPI3_MOSI_M0 / UART9_CTSN_M0
99	GND	Ground	GND	No	1	GND
100	GND	Ground	GND	No	1	GND

Appendix B J2 Pin Summary

J2 has 100 pins. The table lists net names, categories, voltage/properties, default carrier usage and alternate-function counts. See the companion Excel file for complete function names.

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
1	GND	Ground	GND	No	1	GND
2	GND	Ground	GND	No	1	GND
3	SATA30_1_RXP	SATA	Dedicated	Yes	2	SATA30_1_RXP / PCIE20_1_RXP
4	SATA30_0_RXP	SATA	Dedicated	Yes	2	SATA30_0_RXP / PCIE20_0_RXP
5	SATA30_1_RXN	SATA	Dedicated	Yes	2	SATA30_1_RXN / PCIE20_1_RXN
6	SATA30_0_RXN	SATA	Dedicated	Yes	2	SATA30_0_RXN / PCIE20_0_RXN
7	SATA30_1_TXP	SATA	Dedicated	Yes	2	SATA30_1_TXP / PCIE20_1_TXP
8	SATA30_0_TXP	SATA	Dedicated	Yes	2	SATA30_0_TXP / PCIE20_0_TXP
9	SATA30_1_TXN	SATA	Dedicated	Yes	2	SATA30_1_TXN / PCIE20_1_TXN
10	SATA30_0_TXN	SATA	Dedicated	Yes	2	SATA30_0_TXN / PCIE20_0_TXN
11	GND	Ground	GND	No	1	GND
12	GND	Ground	GND	No	1	GND
13	PCIE20_1_REFCLKP	PCIe	Dedicated	Yes	1	PCIE20_1_REFCLKP

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
14	PCIE20_0_REFCLKP	PCle	Dedicated	No	1	PCIE20_0_REFCLKP
15	PCIE20_1_REFCLKN	PCle	Dedicated	Yes	1	PCIE20_1_REFCLKN
16	PCIE20_0_REFCLKN	PCle	Dedicated	No	1	PCIE20_0_REFCLKN
17	GND	Ground	GND	No	1	GND
18	GND	Ground	GND	No	1	GND
19	USB30_2_SSRXN	USB	Dedicated	Yes	3	USB30_2_SSRXN / SATA30_2_RXN / PCIE20_2_RXN
20	PCIE30_PORT0_RX0P	PCle	Dedicated	Yes	1	PCIE30_PORT0_RX0P
21	USB30_2_SSRXN	USB	Dedicated	Yes	3	USB30_2_SSRXN / SATA30_2_RXN / PCIE20_2_RXN
22	PCIE30_PORT0_RX0N	PCle	Dedicated	Yes	1	PCIE30_PORT0_RX0N
23	USB30_2_SSTXP	USB	Dedicated	Yes	3	USB30_2_SSTXP / SATA30_2_TXP / PCIE20_2_TXP
24	PCIE30_PORT0_RX1P	PCle	Dedicated	Yes	1	PCIE30_PORT0_RX1P
25	USB30_2_SSTXN	USB	Dedicated	Yes	3	USB30_2_SSTXN / SATA30_2_TXN / PCIE20_2_TXN
26	PCIE30_PORT0_RX1N	PCle	Dedicated	Yes	1	PCIE30_PORT0_RX1N
27	GND	Ground	GND	No	1	GND
28	GND	Ground	GND	No	1	GND
29	PCIE20_2_REFCLKP	PCle	Dedicated	Yes	1	PCIE20_2_REFCLKP

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
30	PCIE30_PORT0_REF_CLKP	PCle	Dedicated	Yes	1	PCIE30_PORT0_REF_CLKP
31	PCIE20_2_REFCLKN	PCle	Dedicated	Yes	1	PCIE20_2_REFCLKN
32	PCIE30_PORT0_REF_CLKN	PCle	Dedicated	Yes	1	PCIE30_PORT0_REF_CLKN
33	GND	Ground	GND	No	1	GND
34	GND	Ground	GND	No	1	GND
35	PCIE30_PORT1_RX0P	PCle	Dedicated	Yes	1	PCIE30_PORT1_RX0P
36	PCIE30_PORT0_TX0P	PCle	Dedicated	Yes	1	PCIE30_PORT0_TX0P
37	PCIE30_PORT1_RX0N	PCle	Dedicated	Yes	1	PCIE30_PORT1_RX0N
38	PCIE30_PORT0_TX0N	PCle	Dedicated	Yes	1	PCIE30_PORT0_TX0N
39	PCIE30_PORT1_RX1P	PCle	Dedicated	Yes	1	PCIE30_PORT1_RX1P
40	PCIE30_PORT0_TX1P	PCle	Dedicated	Yes	1	PCIE30_PORT0_TX1P
41	PCIE30_PORT1_RX1N	PCle	Dedicated	Yes	1	PCIE30_PORT1_RX1N
42	PCIE30_PORT0_TX1N	PCle	Dedicated	Yes	1	PCIE30_PORT0_TX1N
43	PCIE30_PORT1_TX0P	PCle	Dedicated	Yes	1	PCIE30_PORT1_TX0P
44	GND	Ground	GND	No	1	GND
45	PCIE30_PORT1_TX0N	PCle	Dedicated	Yes	1	PCIE30_PORT1_TX0N
46	GPIO0_A0	GPIO	1.8V	Yes	2	GPIO0_A0 / REFCLK_OUT
47	PCIE30_PORT1_TX1P	PCle	Dedicated	Yes	1	PCIE30_PORT1_TX1P
48	RTC_INT	Other	1.8V	Yes	1	RTC_INT
49	PCIE30_PORT1_TX1N	PCle	Dedicated	Yes	1	PCIE30_PORT1_TX1N

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
50	GPIO0_B2	GPIO	1.8V	Yes	3	GPIO0_B2 / CLK32K_IN / CLK32K_OUT0
51	GND	Ground	GND	No	1	GND
52	GND	Ground	GND	No	1	GND
53	PCIE30_PORT1_REF_CLKP	PCIe	Dedicated	Yes	1	PCIE30_PORT1_REF_CLKP
54	GPIO1_A1	GPIO	3.3V	Yes	7	GPIO1_A1 / UART6_TX_M1 / I2C2_SCL_M4 / DP1_HPDIN_M2 / PCIE30X1_1_WAKEN_M2
55	PCIE30_PORT1_REF_CLKN	PCIe	Dedicated	Yes	1	PCIE30_PORT1_REF_CLKN
56	GPIO1_A0	GPIO	3.3V	Yes	6	GPIO1_A0 / UART6_RX_M1 / I2C2_SDA_M4 / DP0_HPDIN_M2 / PCIE30X1_1_CLKREQN_M2
57	GND	Ground	GND	No	1	GND
58	GND	Ground	GND	No	1	GND
59	GPIO1_C0	GPIO	1.8V	Yes	4	GPIO1_C0 / I2C3_SDA_M0 / UART3_RX_M0 / SPI4_MISO_M0
60	GPIO0_C4	GPIO	3.3V	Yes	7	GPIO0_C4 / PWM2_M0 / I2C4_SDA_M2 / PCIE30X1_0_WAKEN_M0 / PDM0_CLK1_M1
61	GPIO1_C1	GPIO	1.8V	Yes	4	GPIO1_C1 / I2C3_SCL_M0 / UART3_TX_M0 / SPI4_MOSI_M0

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
62	GPIO0_C0	GPIO	3.3V	Yes	7	GPIO0_C0 / PWM1_M0 / I2C2_SDA_M0 / SPI0_MOSI_M0 / PCIE30X1_0_CLKREQN_M0
63	GPIO1_C4	GPIO	1.8V	Yes	5	GPIO1_C4 / PDM0_CLK1_M0 / I2C2_SDA_M3 / PWM11_IR_M2 / SPI4_CS1_M0
64	GPIO0_C5	GPIO	3.3V	Yes	8	GPIO0_C5 / GPU_AVS / I2C4_SCL_M2 / PCIE30X1_0_PERSTN_M0 / I2S1_SDI0_M1
65	GPIO1_C6	GPIO	1.8V	Yes	4	GPIO1_C6 / PDM0_CLK0_M0 / I2C4_SDA_M4 / PWM15_IR_M2
66	GPIO0_B7	GPIO	3.3V	Yes	7	GPIO0_B7 / PWM0_M0 / I2C2_SCL_M0 / SPI0_CS1_M0 / PCIE30X1_1_PERSTN_M0
67	GPIO1_D2	GPIO	1.8V	Yes	8	GPIO1_D2 / I2S0_SDI2 / I2S0_SDO3 / PDM0_SDI2_M0 / I2C1_SCL_M4
68	GPIO0_D3	GPIO	3.3V	Yes	3	GPIO0_D3 / LITCPU_AVS / SPI3_CLK_M2
69	GPIO1_D3	GPIO	1.8V	Yes	7	GPIO1_D3 / I2S0_SDI1 / PDM0_SDI3_M0 / I2C1_SDA_M4 / PWM1_M1
70	GPIO0_D0	GPIO	3.3V	Yes	8	GPIO0_D0 / PWM7_IR_M0 / I2C6_SCL_M0 / SPI3_MISO_M2 /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						PCIE30X4_PERSTN_M0
71	GPIO1_D5	GPIO	1.8V	Yes	3	GPIO1_D5 / PDM0_SDI0_M0 / SPI1_CS1_M2
72	GPIO0_C7	GPIO	3.3V	Yes	8	GPIO0_C7 / PWM6_M0 / I2C6_SDA_M0 / SPI0_MISO_M0 / PCIE30X4_WAKEN_M0
73	GND	Ground	GND	No	1	GND
74	GPIO0_C6	GPIO	3.3V	Yes	8	GPIO0_C6 / NPU_AVS / SPI0_CLK_M0 / PCIE30X4_CLKREQN_M0 / I2S1_SDI1_M1
75	GPIO1_D1	GPIO	1.8V	Yes	7	GPIO1_D1 / I2S0_SDI3 / I2S0_SDO2 / PDM0_SDI1_M0 / I2C7_SDA_M0
76	GND	Ground	GND	No	1	GND
77	GPIO1_D0	GPIO	1.8V	Yes	5	GPIO1_D0 / I2S0_SDO1 / I2C7_SCL_M0 / UART6_TX_M2 / SPI1_MISO_M2
78	GPIO0_B6	GPIO	3.3V	Yes	2	GPIO0_B6 / UART2_RX_M0_DEBUG
79	GND	Ground	GND	No	1	GND
80	GPIO0_B5	GPIO	3.3V	Yes	2	GPIO0_B5 / UART2_TX_M0_DEBUG
81	GPIO1_C2	GPIO	1.8V	Yes	6	GPIO1_C2 / I2S0_MCLK / I2C6_SDA_M1 / PWM3_IR_M2 / UART3_RTSN

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
82	GND	Ground	GND	No	1	GND
83	GPIO1_C3	GPIO	1.8V	Yes	6	GPIO1_C3 / I2S0_SCLK / I2C6_SCL_M1 / PWM7_IR_M2 / UART3_CTSN
84	GPIO0_D1	GPIO	3.3V	Yes	10	GPIO0_D1 / CPU_BIG0_AVS / I2C0_SCL_M2 / SPI0_CS0_M0 / PCIE30X2_CLKREQN_M0
85	GPIO1_C5	GPIO	1.8V	Yes	4	GPIO1_C5 / I2S0_LRCK / I2C2_SCL_M3 / UART4_RTSN
86	GPIO0_D2	GPIO	3.3V	Yes	8	GPIO0_D2 / I2C0_SDA_M2 / SPI3_MOSI_M2 / PCIE30X2_WAKEN_M0 / I2S1_SDO1_M1
87	GPIO1_C7	GPIO	1.8V	Yes	4	GPIO1_C7 / I2S0_SDO0 / I2C4_SCL_M4 / UART4_CTSN
88	GPIO0_D4	GPIO	3.3V	Yes	10	GPIO0_D4 / PWM3_IR_M0 / I2C1_SCL_M2 / SPI3_CS0_M2 / PCIE30X2_PERSTN_M0
89	GPIO1_D4	GPIO	1.8V	Yes	2	GPIO1_D4 / I2S0_SDI0
90	GPIO0_D5	GPIO	3.3V	Yes	8	GPIO0_D5 / CPU_BIG1_AVS / I2C1_SDA_M2 / SPI3_CS1_M2 / I2S1_SDO3_M1
91	GND	Ground	GND	No	1	GND
92	GPIO1_B6	GPIO	3.3V	Yes	7	GPIO1_B6 / UART1_TX_M1 / I2C5_SCL_M3 / MIPI_CAMERA1_CLK_M0 / PCIE30X2_WAKEN_M3

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
93	GPIO1_B4	GPIO	3.3V	Yes	5	GPIO1_B4 / UART7_RX_M2 / PDM1_CLK0_M1 / PCIE30X1_0_PERSTN_M2 / SPI0_CS0_M2
94	GPIO1_B7	GPIO	3.3V	Yes	9	GPIO1_B7 / UART1_RX_M1 / I2C5_SDA_M3 / MIPI_CAMERA2_CLK_M0 / PCIE30X2_PERSTN_M3
95	GPIO1_B5	GPIO	3.3V	Yes	4	GPIO1_B5 / UART7_TX_M2 / PCIE30X1_0_CLKREQN_M2 / SPI0_CS1_M2
96	GPIO1_D6	GPIO	3.3V	Yes	6	GPIO1_D6 / UART1_RTSN_M1 / I2C8_SCL_M2 / MIPI_CAMERA3_CLK_M0 / PWM14_M2
97	GPIO1_B2	GPIO	3.3V	Yes	5	GPIO1_B2 / UART4_RX_M2 / PDM1_SDI3_M1 / PCIE30X4_PERSTN_M3 / SPI0_MOSI_M2
98	GPIO1_D7	GPIO	3.3V	Yes	7	GPIO1_D7 / UART1_CTSN_M1 / I2C8_SDA_M2 / MIPI_CAMERA4_CLK_M0 / PCIE30X2_CLKREQN_M3
99	GPIO1_B3	GPIO	3.3V	Yes	6	GPIO1_B3 / UART4_TX_M2 / PDM1_CLK1_M1 / PCIE30X1_0_WAKEN_M2 / SPI0_CLK_M2
100	GND	Ground	GND	No	1	GND

Appendix C J3 Pin Summary

J3 has 100 pins. The table lists net names, categories, voltage/properties, default carrier usage and alternate-function counts. See the companion Excel file for complete function names.

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
1	GND	Ground	GND	No	1	GND
2	GND	Ground	GND	No	1	GND
3	/	Unused	Dedicated	Yes	1	MIPI_DPHY0_RX_D3P
4	GPIO4_A6	GPIO	3.3V	Yes	8	GPIO4_A6 / CIF_D6 / BT1120_D6 / PCIE30X2_CLKREQN_M1 / I2S1_SDI1_M0
5	MIPI_CPHY0_RX_TRIO2_C	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO2_C / MIPI_DPHY0_RX_D3N
6	GPIO4_A7	GPIO	3.3V	Yes	7	GPIO4_A7 / CIF_D7 / BT1120_D7 / PCIE30X2_WAKEN_M1 / I2S1_SDI2_M0
7	MIPI_CPHY0_RX_TRIO2_B	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO2_B / MIPI_DPHY0_RX_D2P
8	GPIO4_B0	GPIO	3.3V	Yes	8	GPIO4_B0 / CIF_CLKIN / BT1120_CLKOUT / PCIE30X2_PERSTN_M1 / I2S1_SDI3_M0
9	MIPI_CPHY0_RX_TRIO2_A	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO2_A / MIPI_DPHY0_RX_D2N
10	GND	Ground	GND	No	1	GND

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
11	GND	Ground	GND	No	1	GND
12	GPIO4_A0	GPIO	3.3V	Yes	7	GPIO4_A0 / CIF_D0 / BT1120_D0 / PCIE30X1_1_CLKREQN_M1 / I2S1_MCLK_M0
13	MIPI_CPHY0_RX_TRIO1_C	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO1_C / MIPI_DPHY0_RX_CLKP
14	GPIO4_A1	GPIO	3.3V	Yes	7	GPIO4_A1 / CIF_D1 / BT1120_D1 / PCIE30X1_1_WAKEN_M1 / I2S1_SCLK_M0
15	MIPI_CPHY0_RX_TRIO1_B	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO1_B / MIPI_DPHY0_RX_CLKN
16	GPIO4_A2	GPIO	3.3V	Yes	6	GPIO4_A2 / CIF_D2 / BT1120_D2 / PCIE30X1_1_PERSTN_M1 / I2S1_LRCK_M0
17	GND	Ground	GND	No	1	GND
18	GND	Ground	GND	No	1	GND
19	MIPI_CPHY0_RX_TRIO1_A	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO1_A / MIPI_DPHY0_RX_D1P
20	GPIO4_B4	GPIO	3.3V	Yes	9	GPIO4_B4 / CIF_CLKOUT / BT1120_D10 / PCIE30X4_CLKREQN_M1 / I2S1_SDO3_M0
21	MIPI_CPHY0_RX_TRIO0_C	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO0_C / MIPI_DPHY0_RX_D1N

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
22	GPIO4_B5	GPIO	3.3V	Yes	8	GPIO4_B5 / BT1120_D11 / PCIE30X4_WAKEN_M1 / HDMI_RX_CEC_M0 / UART9_RX_M1
23	MIPI_CPHY0_RX_TRIO0_B	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO0_B / MIPI_DPHY0_RX_D0P
24	GPIO4_B6	GPIO	3.3V	Yes	8	GPIO4_B6 / BT1120_D12 / PCIE30X4_PERSTN_M1 / HDMI_RX_HPDOOUT_M0 / I2C5_SCL_M1
25	MIPI_CPHY0_RX_TRIO0_A	MIPI	Dedicated	Yes	2	MIPI_CPHY0_RX_TRIO0_A / MIPI_DPHY0_RX_D0N
26	GND	Ground	GND	No	1	GND
27	GND	Ground	GND	No	1	GND
28	GPIO4_B3	GPIO	3.3V	Yes	9	GPIO4_B3 / CIF_VSYNC / BT1120_D9 / PCIE20X1_2_BUTTON_RSTN / I2S1_SDO2_M0
29	/	Unused	Dedicated	Yes	1	MIPI_DPHY0_TX_D3P
30	GPIO4_B2	GPIO	3.3V	Yes	10	GPIO4_B2 / CIF_HREF / BT1120_D8 / PCIE30X1_1_BUTTON_RSTN / I2S1_SDO1_M0
31	MIPI_CPHY0_TX_TRIO2_C	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO2_C / MIPI_DPHY0_TX_D3N
32	GND	Ground	GND	No	1	GND
33	MIPI_CPHY0_TX_TRIO2_B	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO2_B /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						MIPI_DPHY0_TX_D2P
34	GPIO3_C5	GPIO	3.3V	Yes	8	GPIO3_C5 / CIF_D9 / HDMI_TX1_SDA_M1 / SPI3_CS1_M3 / FSPI_CS1N_M2
35	MIPI_CPHY0_TX_TRIO2_A	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO2_A / MIPI_DPHY0_TX_D2N
36	GPIO3_C4	GPIO	3.3V	Yes	8	GPIO3_C4 / CIF_D8 / HDMI_TX1_CEC_M2 / SPI3_CS0_M3 / FSPI_CS0N_M2
37	GND	Ground	GND	No	1	GND
38	GND	Ground	GND	No	1	GND
39	MIPI_CPHY0_TX_TRIO1_C	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO1_C / MIPI_DPHY0_TX_CLKP
40	SARADC_IN7	ADC	1.8V	Yes	1	SARADC_IN7
41	MIPI_CPHY0_TX_TRIO1_B	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO1_B / MIPI_DPHY0_TX_CLKN
42	SARADC_IN6	ADC	1.8V	Yes	1	SARADC_IN6
43	GND	Ground	GND	No	1	GND
44	SARADC_IN5	ADC	1.8V	Yes	1	SARADC_IN5
45	MIPI_CPHY0_TX_TRIO1_A	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO1_A / MIPI_DPHY0_TX_D1P
46	SARADC_IN4	ADC	1.8V	Yes	1	SARADC_IN4
47	MIPI_CPHY0_TX_TRIO0_C	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO0_C / MIPI_DPHY0_TX_D1N

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
48	SARADC_IN3	ADC	1.8V	Yes	1	SARADC_IN3
49	MIPI_CPHY0_TX_TRIO0_B	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO0_B / MIPI_DPHY0_TX_D0P
50	RECOVERY_KEY	Other	1.8V	Yes	1	RECOVERY_KEY
51	MIPI_CPHY0_TX_TRIO0_A	MIPI	Dedicated	Yes	2	MIPI_CPHY0_TX_TRIO0_A / MIPI_DPHY0_TX_D0N
52	SARADC_IN0_BOOT	ADC	1.8V	Yes	1	SARADC_IN0_BOOT
53	GND	Ground	GND	No	1	GND
54	GND	Ground	GND	No	1	GND
55	/	Unused	Dedicated	Yes	1	MIPI_DPHY1_TX_D3P
56	GPIO4_B7	GPIO	3.3V	Yes	6	GPIO4_B7 / BT1120_D13 / PCIE20X1_2_CLKREQN_M1 / HDMI_TX0_SCL_M0 / I2C5_SDA_M1
57	MIPI_CPHY1_TX_TRIO2_C	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO2_C / MIPI_DPHY1_TX_D3N
58	GPIO4_C0	GPIO	3.3V	Yes	6	GPIO4_C0 / BT1120_D14 / PCIE20X1_2_WAKEN_M1 / HDMI_TX0_SDA_M0 / I2C8_SCL_M3
59	MIPI_CPHY1_TX_TRIO2_B	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO2_B / MIPI_DPHY1_TX_D2P
60	GPIO4_C1	GPIO	3.3V	Yes	8	GPIO4_C1 / BT1120_D15 / PCIE20X1_2_PERSTN_M1 / HDMI_TX0_CEC_M0 / I2C8_SDA_M3

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
61	MIPI_CPHY1_TX_TRIO2_A	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO2_A / MIPI_DPHY1_TX_D2N
62	GND	Ground	GND	No	1	GND
63	MIPI_CPHY1_TX_TRIO1_C	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO1_C / MIPI_DPHY1_TX_CLKP
64	DP0_TX3P	Display	Dedicated	Yes	2	DP0_TX3P / TYPEC0_SSTX2P
65	MIPI_CPHY1_TX_TRIO1_B	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO1_B / MIPI_DPHY1_TX_CLKN
66	DP0_TX3N	Display	Dedicated	Yes	2	DP0_TX3N / TYPEC0_SSTX2N
67	MIPI_CPHY1_TX_TRIO1_A	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO1_A / MIPI_DPHY1_TX_D1P
68	DP0_TX2P	Display	Dedicated	Yes	2	DP0_TX2P / TYPEC0_SSRX2P
69	MIPI_CPHY1_TX_TRIO0_C	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO0_C / MIPI_DPHY1_TX_D1N
70	DP0_TX2N	Display	Dedicated	Yes	2	DP0_TX2N / TYPEC0_SSRX2N
71	MIPI_CPHY1_TX_TRIO0_B	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO0_B / MIPI_DPHY1_TX_D0P
72	GND	Ground	GND	No	1	GND
73	MIPI_CPHY1_TX_TRIO0_A	MIPI	Dedicated	Yes	2	MIPI_CPHY1_TX_TRIO0_A / MIPI_DPHY1_TX_D0N
74	DP0_TX1P	Display	Dedicated	Yes	2	DP0_TX1P / TYPEC0_SSTX1P
75	GND	Ground	GND	No	1	GND
76	DP0_TX1N	Display	Dedicated	Yes	2	DP0_TX1N / TYPEC0_SSTX1N

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
77	/	Unused	Dedicated	Yes	1	MIPI_DPHY1_RX_D3P
78	DP0_TX0P	Display	Dedicated	Yes	2	DP0_TX0P / TYPEC0_SSRX1P
79	MIPI_CPHY1_RX_TRIO2_C	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO2_C / MIPI_DPHY1_RX_D3N
80	DP0_TX0N	Display	Dedicated	Yes	2	DP0_TX0N / TYPEC0_SSRX1N
81	MIPI_CPHY1_RX_TRIO2_B	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO2_B / MIPI_DPHY1_RX_D2P
82	GND	Ground	GND	No	1	GND
83	MIPI_CPHY1_RX_TRIO2_A	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO2_A / MIPI_DPHY1_RX_D2N
84	DP0_AUXP	Display	Dedicated	Yes	2	DP0_AUXP / TYPEC0_SBU1
85	MIPI_CPHY1_RX_TRIO1_C	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO1_C / MIPI_DPHY1_RX_CLKP
86	DP0_AUXN	Display	Dedicated	Yes	2	DP0_AUXN / TYPEC0_SBU2
87	MIPI_CPHY1_RX_TRIO1_B	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO1_B / MIPI_DPHY1_RX_CLKN
88	GND	Ground	GND	No	1	GND
89	MIPI_CPHY1_RX_TRIO1_A	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO1_A / MIPI_DPHY1_RX_D1P
90	TYPEC0_USB20_OTG_ID	USB	Dedicated	Yes	1	TYPEC0_USB20_OTG_ID
91	MIPI_CPHY1_RX_TRIO0_C	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO0_C / MIPI_DPHY1_RX_D1N
92	TYPEC0_USB20_VBUSDET	USB	Dedicated	Yes	1	TYPEC0_USB20_VBUSDET

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
93	MIPI_CPHY1_RX_TRIO0_B	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO0_B / MIPI_DPHY1_RX_D0P
94	GND	Ground	GND	No	1	GND
95	MIPI_CPHY1_RX_TRIO0_A	MIPI	Dedicated	Yes	2	MIPI_CPHY1_RX_TRIO0_A / MIPI_DPHY1_RX_D0N
96	TYPEC0_USB20_OTG_DP	USB	Dedicated	Yes	1	TYPEC0_USB20_OTG_DP
97	GND	Ground	GND	No	1	GND
98	TYPEC0_USB20_OTG_DM	USB	Dedicated	Yes	1	TYPEC0_USB20_OTG_DM
99	GND	Ground	GND	No	1	GND
100	GND	Ground	GND	No	1	GND

Appendix D J4 Pin Summary

J4 has 100 pins. The table lists net names, categories, voltage/properties, default carrier usage and alternate-function counts. See the companion Excel file for complete function names.

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
1	GND	Ground	GND	No	1	GND
2	GND	Ground	GND	No	1	GND
3	EDP_TX1_D2P	Display	Dedicated	Yes	2	EDP_TX1_D2P / HDMI_TX1_D2P
4	DP1_AUXP	Display	Dedicated	No	2	DP1_AUXP / TYPEC1_SBU1
5	EDP_TX1_D2N	Display	Dedicated	Yes	2	EDP_TX1_D2N / HDMI_TX1_D2N
6	DP1_AUXN	Display	Dedicated	No	2	DP1_AUXN / TYPEC1_SBU2
7	EDP_TX1_D1P	Display	Dedicated	Yes	2	EDP_TX1_D1P / HDMI_TX1_D1P
8	GND	Ground	GND	No	1	GND
9	EDP_TX1_D1N	Display	Dedicated	Yes	2	EDP_TX1_D1N / HDMI_TX1_D1N
10	TYPEC1_USB20_OTG_DP	USB	Dedicated	Yes	1	TYPEC1_USB20_OTG_DP
11	EDP_TX1_D0P	Display	Dedicated	Yes	2	EDP_TX1_D0P / HDMI_TX1_D0P
12	TYPEC1_USB20_OTG_DM	USB	Dedicated	Yes	1	TYPEC1_USB20_OTG_DM
13	EDP_TX1_D0N	Display	Dedicated	Yes	2	EDP_TX1_D0N / HDMI_TX1_D0N
14	GND	Ground	GND	No	1	GND

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
15	EDP_TX1_D3P	Display	Dedicated	Yes	2	EDP_TX1_D3P / HDMI_TX1_D3P
16	TYPEC1_USB20_OTG_ID	USB	Dedicated	No	1	TYPEC1_USB20_OTG_ID
17	EDP_TX1_D3N	Display	Dedicated	Yes	2	EDP_TX1_D3N / HDMI_TX1_D3N
18	TYPEC1_USB20_VBUSDET	USB	Dedicated	Yes	1	TYPEC1_USB20_VBUSDET
19	GND	Ground	GND	No	1	GND
20	GND	Ground	GND	No	1	GND
21	EDP_TX1_AUXP	Display	Dedicated	Yes	2	EDP_TX1_AUXP / HDMI_TX1_SBDP
22	DP1_TX3P	Display	Dedicated	No	2	DP1_TX3P / TYPEC1_SSTX2P
23	EDP_TX1_AUXN	Display	Dedicated	Yes	2	EDP_TX1_AUXN / HDMI_TX1_SBDN
24	DP1_TX3N	Display	Dedicated	No	2	DP1_TX3N / TYPEC1_SSTX2N
25	GND	Ground	GND	No	1	GND
26	DP1_TX2P	Display	Dedicated	No	2	DP1_TX2P / TYPEC1_SSRX2P
27	EDP_TX0_D2P	Display	Dedicated	Yes	2	EDP_TX0_D2P / HDMI_TX0_D2P
28	DP1_TX2N	Display	Dedicated	No	2	DP1_TX2N / TYPEC1_SSRX2N
29	EDP_TX0_D2N	Display	Dedicated	Yes	2	EDP_TX0_D2N / HDMI_TX0_D2N
30	GND	Ground	GND	No	1	GND
31	EDP_TX0_D1P	Display	Dedicated	Yes	2	EDP_TX0_D1P /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						HDMI_TX0_D1P
32	DP1_TX1P	Display	Dedicated	Yes	2	DP1_TX1P / TYPEC1_SSTX1P
33	EDP_TX0_D1N	Display	Dedicated	Yes	2	EDP_TX0_D1N / HDMI_TX0_D1N
34	DP1_TX1N	Display	Dedicated	Yes	2	DP1_TX1N / TYPEC1_SSTX1N
35	EDP_TX0_D0P	Display	Dedicated	Yes	2	EDP_TX0_D0P / HDMI_TX0_D0P
36	DP1_TX0P	Display	Dedicated	Yes	2	DP1_TX0P / TYPEC1_SSRX1P
37	EDP_TX0_D0N	Display	Dedicated	Yes	2	EDP_TX0_D0N / HDMI_TX0_D0N
38	DP1_TX0N	Display	Dedicated	Yes	2	DP1_TX0N / TYPEC1_SSRX1N
39	EDP_TX0_D3P	Display	Dedicated	Yes	2	EDP_TX0_D3P / HDMI_TX0_D3P
40	GND	Ground	GND	No	1	GND
41	EDP_TX0_D3N	Display	Dedicated	Yes	2	EDP_TX0_D3N / HDMI_TX0_D3N
42	GPIO3_A6	GPIO	3.3V	Yes	4	GPIO3_A6 / ETH1_REFCLKO_25M / I2C4_SCL_M0 / MIPI_CAMERA1_CLK_M1
43	GND	Ground	GND	No	1	GND
44	GPIO3_B2	GPIO	3.3V	Yes	5	GPIO3_B2 / GMAC1_TXER / I2S2_SDI_M1 / UART2_RX_M2 / PWM3_IR_M1
45	EDP_TX0_AUXP	Display	Dedicated	Yes	2	EDP_TX0_AUXP /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						HDMI_TX0_SBDP
46	GPIO3_B7	GPIO	3.3V	Yes	5	GPIO3_B7 / GMAC1_PTP_REF_CLK / HDMI_TX1_HPD_M1 / SPI1_MOSI_M1 / I2C3_SCL_M1
47	EDP_TX0_AUXN	Display	Dedicated	Yes	2	EDP_TX0_AUXN / HDMI_TX0_SBDN
48	GPIO3_C0	GPIO	3.3V	Yes	5	GPIO3_C0 / GMAC1_PPSTRIG / SPI1_MISO_M1 / I2C3_SDA_M1 / UART7_TX_M1
49	GND	Ground	GND	No	1	GND
50	GPIO3_C1	GPIO	3.3V	Yes	5	GPIO3_C1 / GMAC1_PPSCCLK / SPI1_CLK_M1 / UART7_RX_M1 / PCIE30X2_BUTTON_RSTN
51	HDMI_RX_D2P	Display	Dedicated	Yes	1	HDMI_RX_D2P
52	GPIO3_C6	GPIO	3.3V	No	5	GPIO3_C6 / CIF_D10 / HDMI_TX1_SCL_M1 / SPI3_MISO_M3 / PCIE30X4_PERSTN_M2
53	HDMI_RX_D2N	Display	Dedicated	Yes	1	HDMI_RX_D2N
54	GPIO3_C7	GPIO	3.3V	Yes	6	GPIO3_C7 / CIF_D11 / HDMI_TX0_SCL_M2 / SPI3_MOSI_M3 / I2C5_SCL_M0
55	HDMI_RX_D1P	Display	Dedicated	Yes	1	HDMI_RX_D1P

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
56	GPIO3_D0	GPIO	3.3V	Yes	8	GPIO3_D0 / CIF_D12 / HDMI_TX0_SDA_M2 / SPI3_CLK_M3 / I2C5_SDA_M0
57	HDMI_RX_D1N	Display	Dedicated	Yes	1	HDMI_RX_D1N
58	GPIO3_D5	GPIO	3.3V	Yes	7	GPIO3_D5 / MCU_JTAG_TMS_M1 / DP1_HPDIN_M0 / SPI0_CS1_M3 / UART9_TX_M2
59	HDMI_RX_D0P	Display	Dedicated	Yes	1	HDMI_RX_D0P
60	GPIO4_A3	GPIO	3.3V	Yes	5	GPIO4_A3 / CIF_D3 / BT1120_D3 / PCIE30X1_0_CLKREQN_M1 / UART0_TX_M2
61	HDMI_RX_D0N	Display	Dedicated	Yes	1	HDMI_RX_D0N
62	GPIO4_A4	GPIO	3.3V	Yes	7	GPIO4_A4 / CIF_D4 / BT1120_D4 / PCIE30X1_0_WAKEN_M1 / I2C3_SCL_M2
63	HDMI_RX_CLKP	Display	Dedicated	Yes	1	HDMI_RX_CLKP
64	GPIO4_A5	GPIO	3.3V	Yes	8	GPIO4_A5 / CIF_D5 / BT1120_D5 / PCIE30X1_0_PERSTN_M1 / I2S1_SDI0_M0
65	HDMI_RX_CLKN	Display	Dedicated	Yes	1	HDMI_RX_CLKN
66	GPIO4_B1	GPIO	3.3V	Yes	9	GPIO4_B1 / MIPI_CAMERA0_CLK_M0 / PCIE30X1_0_BUTTON_RSTN / I2S1_SDO0_M0 /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						I2C6_SCL_M3
67	GND	Ground	GND	No	1	GND
68	GND	Ground	GND	No	1	GND
69	GPIO4_D0	GPIO	Dedicated	Yes	7	GPIO4_D0 / SDMMC_D0 / UART2_TX_M1 / JTAG_TCK_M1 / PDM1_SDI3_M0
70	GPIO3_D2	GPIO	3.3V	Yes	7	GPIO3_D2 / CIF_D14 / HDMI_RX_SCL_M1 / SPI0_MOSI_M3 / I2C7_SCL_M2
71	GPIO4_D1	GPIO	Dedicated	Yes	7	GPIO4_D1 / SDMMC_D1 / UART2_RX_M1 / JTAG_TMS_M1 / PDM1_SDI2_M0
72	GPIO3_D3	GPIO	3.3V	Yes	8	GPIO3_D3 / CIF_D15 / HDMI_RX_SDA_M1 / SPI0_CLK_M3 / I2C7_SDA_M2
73	GPIO4_D2	GPIO	Dedicated	Yes	6	GPIO4_D2 / SDMMC_D2 / UART5_CTSN_M0 / JTAG_TCK_M0 / PDM1_SDI1_M0
74	GPIO3_D1	GPIO	3.3V	Yes	7	GPIO3_D1 / CIF_D13 / HDMI_RX_CEC_M1 / SPI0_MISO_M3 / UART4_TX_M1
75	GPIO4_D3	GPIO	Dedicated	Yes	7	GPIO4_D3 / SDMMC_D3 / UART5_RTSN_M0 / JTAG_TMS_M0 /

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						PDM1_SDI0_M0
76	GPIO3_D4	GPIO	3.3V	Yes	7	GPIO3_D4 / MCU_JTAG_TCK_M1 / HDMI_TX0_HPD_M1 / HDMI_RX_HPDP0UT_M1 / SPI0_CS0_M3
77	GPIO4_D5	GPIO	Dedicated	Yes	7	GPIO4_D5 / SDMMC_CLK / UART5_TX_M0 / MCU_JTAG_TMS_M0 / PDM1_CLK0_M0
78	GND	Ground	GND	No	1	GND
79	GPIO4_D4	GPIO	Dedicated	Yes	7	GPIO4_D4 / SDMMC_CMD / UART5_RX_M0 / MCU_JTAG_TCK_M0 / PDM1_CLK1_M0
80	USB20_HOST1_DP	USB	Dedicated	Yes	1	USB20_HOST1_DP
81	GPIO0_A4	GPIO	Dedicated	Yes	2	GPIO0_A4 / SDMMC_DET
82	USB20_HOST1_DM	USB	Dedicated	Yes	1	USB20_HOST1_DM
83	GND	Ground	GND	No	1	GND
84	GND	Ground	GND	No	1	GND
85	GPIO1_A2	GPIO	3.3V	Yes	6	GPIO1_A2 / UART6_RTSN_M1 / I2C4_SDA_M3 / VOP_POST_EMPTY / SPI4_CLK_M2
86	USB20_HOST0_DP	USB	Dedicated	Yes	1	USB20_HOST0_DP
87	GPIO1_A3	GPIO	3.3V	Yes	6	GPIO1_A3 / UART6_CTSN_M1

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
						/ I2C4_SCL_M3 / HDMI_TX1_SDA_M2 / SPI4_CS0_M2
88	USB20_HOST0_DM	USB	Dedicated	Yes	1	USB20_HOST0_DM
89	GPIO1_A4	GPIO	3.3V	Yes	3	GPIO1_A4 / HDMI_TX1_SCL_M2 / SPI2_MISO_M0
90	GND	Ground	GND	No	1	GND
91	GPIO1_A7	GPIO	3.3V	Yes	5	GPIO1_A7 / PDM1_SDI0_M1 / PCIE30X1_1_PERSTN_M2 / SPI2_CS0_M0 / PWM3_IR_M3
92	GPIO1_A5	GPIO	3.3V	Yes	3	GPIO1_A5 / HDMI_TX0_HPD_M0 / SPI2_MOSI_M0
93	GPIO1_B0	GPIO	3.3V	Yes	4	GPIO1_B0 / PDM1_SDI1_M1 / PCIE30X4_CLKREQN_M3 / SPI2_CS1_M0
94	GPIO1_A6	GPIO	3.3V	Yes	3	GPIO1_A6 / HDMI_TX1_HPD_M0 / SPI2_CLK_M0
95	GPIO1_B1	GPIO	3.3V	Yes	4	GPIO1_B1 / PDM1_SDI2_M1 / PCIE30X4_WAKEN_M3 / SPI0_MISO_M2
96	GND	Ground	GND	No	1	GND
97	GND	Ground	GND	No	1	GND
98	GND	Ground	GND	No	1	GND

Pin	Net Name	Category	Level / Property	Carrier Default	Mux Count	Main Alternate Functions
99	GND	Ground	GND	No	1	GND
100	GND	Ground	GND	No	1	GND