

YC-CORE-RK3576-LPD4

Product Specification

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Company Profile

Shenzhen Yuchuang Xingye Technology Co., Ltd. is located in Bantian Subdistrict, Longgang District, Shenzhen, Guangdong Province, China. The company specializes in the design, research and development, production, sales and technical services of embedded system-on-modules, development boards and related hardware and software products. It focuses on embedded product design, hardware and software adaptation, and product quality assurance, serving applications such as edge computing, industrial control, multimedia and the Internet of Things.

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Revision History

Version	Date	Author	Remarks
1.0	2026-10-09	Yang Yunfeng	Initial release

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Chapter 1 System-on-Module Overview

The YC-CORE-RK3576-LPD4 is a system-on-module based on the Rockchip RK3576 processor and built entirely with domestically sourced components in China. Its compact 38 mm x 38 mm design provides up to 240 pins and supports a single 5 V supply, simplifying system power design. The module uses a 12-layer PCB with a lead-free immersion-gold finish to ensure signal integrity and excellent EMC performance. An integrated RK806S-5 power-management IC improves system integration and energy efficiency.

The RK3576 processor uses a big.LITTLE architecture with four Cortex-A72 cores (2.2 GHz) and four Cortex-A53 cores (1.8 GHz), together with an independent NEON coprocessor. It is suitable for ARM PCs, edge computing and multimedia devices. Its multimedia engine supports H.265/VP9/AV1 decoding at 4K@120 fps and H.264/H.265 encoding at 4K@60 fps, and integrates a high-performance JPEG encoder/decoder and image pre-processing/post-processing units.

For graphics processing, the RK3576 incorporates a Mali-G52 GPU with full support for OpenGL ES 3.2, OpenCL 2.0 and Vulkan 1.1. A dedicated 2D acceleration engine delivers a smooth visual experience. The integrated 16 MP ISP supports advanced image-processing algorithms including HDR, 3A and 3DNR for high-end imaging applications.

The integrated NPU provides strong AI computing capabilities and supports mixed-precision operations including INT4, INT8 and FP16. It efficiently runs models from mainstream AI frameworks such as TensorFlow and PyTorch. High-performance LPDDR4 memory provides sufficient bandwidth for a wide range of applications. This solution is particularly suitable for embedded applications requiring high-performance computing, AI inference and multimedia processing. The RK3576 supports high-performance LPDDR4 to deliver the memory bandwidth required by demanding applications. See Figures 1-1 and 1-2.

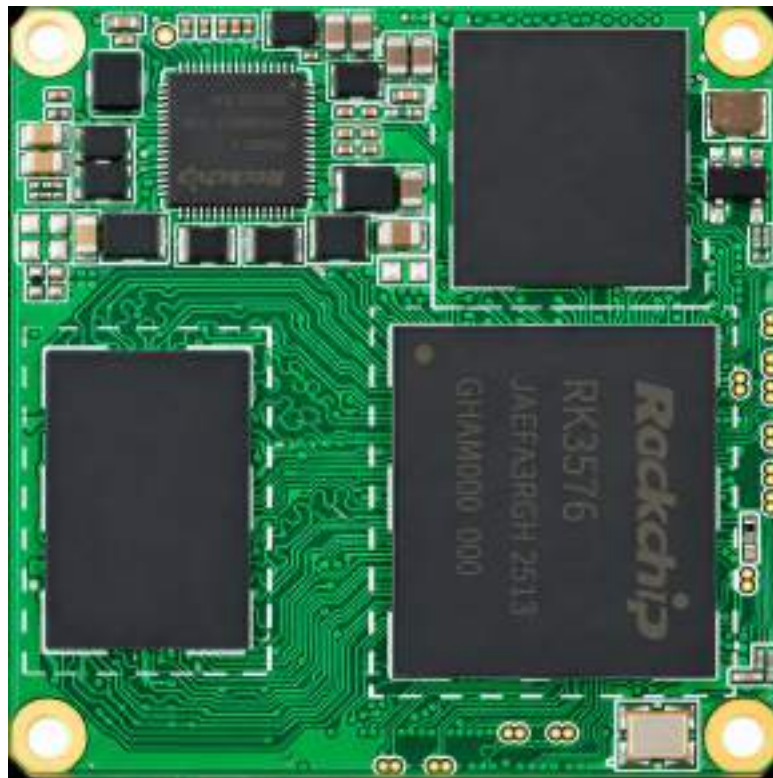


Figure 1-1 Front view of the system-on-module

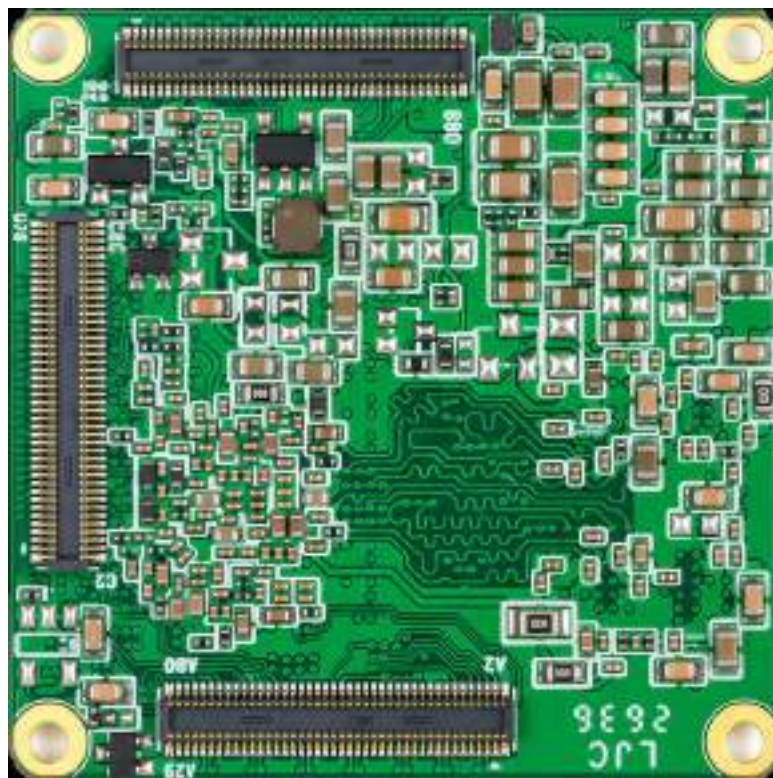


Figure 1-2 Rear view of the system-on-module

Chapter 2 Typical Applications

- Embedded edge computing
- Personal mobile Internet devices
- Multimedia products
- Smart IoT gateways
- Electric power industry and new-energy charging
- Medical electronics
- Cloud terminals
- Smart manufacturing, smart cities and smart transportation
- Industrial automation and security
- Industrial computers and tablets

Chapter 3 Hardware and Software Specifications

The RK3576 processor block diagram is shown in Figure 3-1. The system-on-module hardware block diagram is shown in Figure 3-2.

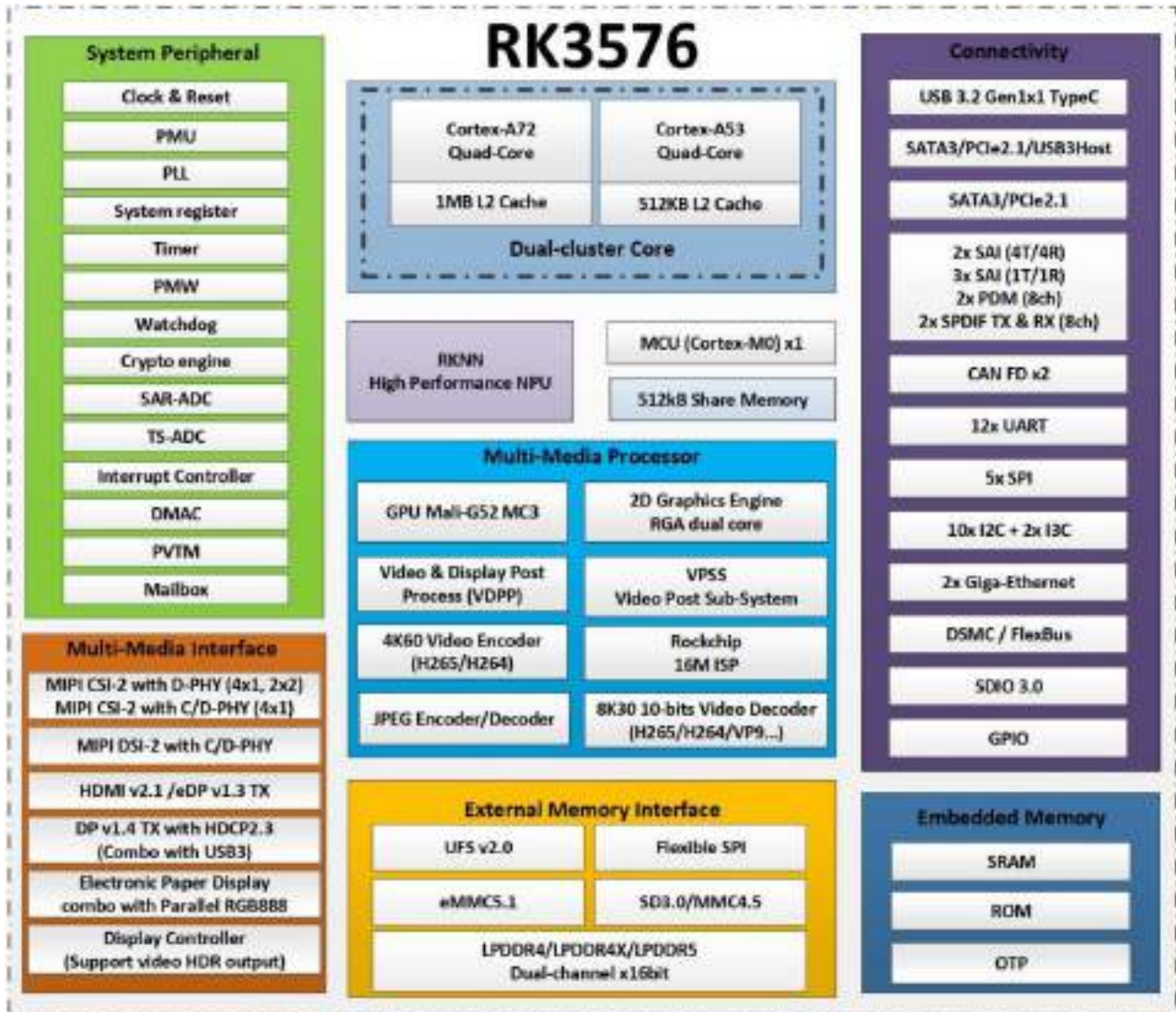


Figure 3-1 RK3576 processor block diagram

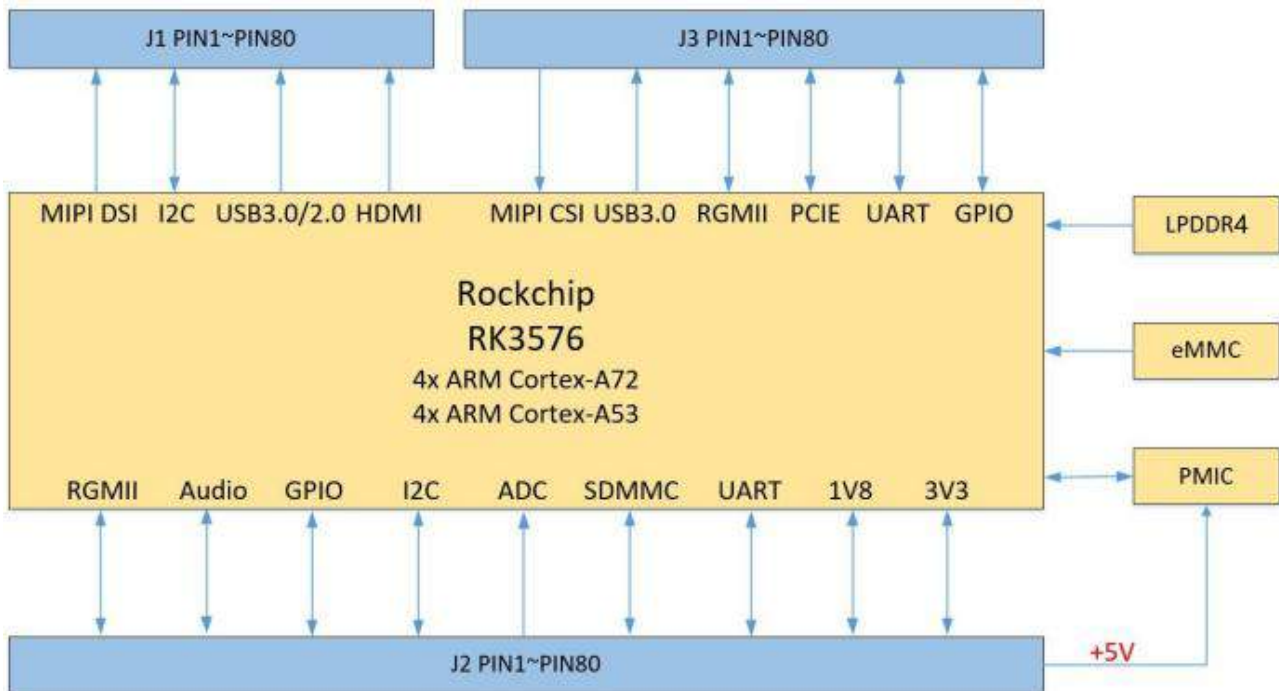


Figure 3-2 System-on-module hardware block diagram

Hardware Specifications

Hardware specifications are listed in Table 3-1.

Table 3-1 Hardware Specifications

Item	Description
CPU	Quad-core Cortex-A72 processor + quad-core Cortex-A53 processor
Clock Frequency	2.2 GHz
Memory	4 GB LPDDR4
eMMC	64 GB eMMC
Multimedia Processing	H.265, VP9, AVS2 and AV1 decoding at 4K@120 fps; H.264 decoding at 4K@60 fps. H.264 and H.265 encoding at 4K@60 fps; high-quality JPEG encoder/decoder.
Graphics Processor	ARM Mali-G52-MC3
NPU	Integrated independent NPU; 6 TOPS at INT8
Dimensions	38 mm x 38 mm
Connection	BTB connectors, 240 pins
Temperature	0°C to +80°C
Operating Voltage	5 V
Operating Systems	Linux, Ubuntu, Android

Hardware resources are listed in Table 3-2 on the following pages.

Hardware Resources

Table 3-2 Hardware Resources (1 of 3)

Resource	Quantity	Description
SDMMC	Up to 2	Supports SDIO 3.0 and MMC V4.51; 4-bit data bus. Supports SDR104 mode at up to 200 MHz. Note: Only SDMMC0 supports system boot; it is assigned to the SD card by default. SD cards can program firmware when eMMC/UFS is blank and update eMMC/UFS firmware after booting from eMMC/UFS. Configure VCCIO_SD_S0 to 1.8 V or 3.3 V according to the peripheral and operating mode. SDMMC1 is 3.3 V. Some pins are multiplexed.
SARADC	Up to 7	12-bit resolution, 1 MS/s; input voltage range: 0-1.8 V. Note: SARADC_VIN0_BOOT is dedicated to SYSTEMBOOT boot-order configuration and cannot be used for other functions. SARADC_VIN1 is the default key-input sampling port and is also the Recovery-mode key (cannot be changed). SARADC_VIN2 is the board hardware ID and is not exposed. SARADC_VIN3 is multiplexed for audio detection. SARADC_VIN4-7 are directly available.
USB	Up to 2	Note: USB2_OTG0 is the default RK3576 firmware-programming port and must be reserved in the application. USB3 and USB2.0 OTG must both operate as Device or both as HOST. USB3 OTG0 SuperSpeed signals (5 Gbps) are multiplexed with DP 1.4. USB3 OTG1 SuperSpeed signals (5 Gbps) are multiplexed with PCIe1 or SATA1. USB is unavailable when configured for PCIe or SATA.
SATA	Up to 2	Supports SATA port-multiplier functionality, with up to 5 devices per port. Supports SATA 1.5/3.0/6.0 Gb/s and eSATA. Note: SATA0 is multiplexed with PCIe0. SATA1 is multiplexed with PCIe1 or USB3_OTG1.
PCIe	Up to 2	Two PCIe 2.1 controllers, both supporting RC mode only. Note: PCIe0 is multiplexed with SATA0. PCIe1 is multiplexed with SATA1 or USB3_OTG1.
MIPI DPHY CSI RX	Up to 4	Two MIPI DPHY CSI RX ports supporting 2/4-lane MIPI-CSI mode. Note: Supports two 4-lane cameras or four 2-lane cameras.
CIF	Up to 1	One DVP interface, up to 16 bits; supports 8/10/12/16 bits. Note: 3.3 V interface. Some pins are multiplexed.

Hardware Resources (Continued)

Table 3-2 Hardware Resources (2 of 3)

Resource	Quantity	Description
HDMI TX	Up to 1	Supports up to HDMI 2.1 and 4K@120 Hz. Supports HDMI FRL mode with backward compatibility for HDMI TMDS mode. Note: Multiplexed with the eDP controller.
eDP	Up to 1	Supports up to eDP 3.1 and 4K@60 Hz. Supports 1/2/4-lane modes; lane swap is not supported. Note: Multiplexed with the eDP controller (as stated in the source).
MIPI DCPHY CSI TX	Up to 1	One MIPI DCPHY CSI RX port supporting 1/2/3/4-lane MIPI-DPHY mode or 0/1/2-trio MIPI-CPHY mode. Note: Cannot be split into 2-lane + 2-lane mode. TX and RX of the MIPI DCPHY Combo PHY must both be configured in DPHY TX/RX modes, or both in CPHY TX/RX modes.
DP	Up to 1	Supports up to eDP 3.1 and 4K@120 Hz (as stated in the source). Supports 1/2/4-lane modes and lane swap. Note: Multiplexed with the SuperSpeed signals of USB3 OTG0.
EBC	Up to 1	Supports 8-bit/16-bit output and up to 32 grayscale levels. Maximum resolution: 2560 x 1920@85 Hz. Note: Some pins are multiplexed.
Audio	Up to 9	5 SAI groups supporting master/slave mode, 8-32-bit word lengths and sample rates up to 48 kHz. 2 PDM groups in master mode supporting 8-channel input, 16-32-bit word lengths and sample rates up to 192 kHz. 2 SPDIF TX groups; 1 DSM PWM Audio group. Note: 4 ASRC (asynchronous sample-rate converter) modules are provided for audio sample-rate conversion. 1.8 V/3.3 V interfaces. Some pins are multiplexed.
Ethernet	Up to 2	Two RGMII interfaces supporting 10/100/1000 Mbps. Note: 3.3 V RGMII/RMII interfaces. Some pins are multiplexed.
UART	Up to 12	Maximum baud rate: 8 Mbps. Note: 1.8 V/3.3 V interfaces. Some pins are multiplexed.
I3C	Up to 2	Supports 7-bit and 10-bit addressing, up to 12.5 Mbit/s. Compatible with I2C at up to 400 Kbit/s. Note: 1.8 V/3.3 V interfaces. Some pins are multiplexed.

Hardware Resources (Continued)

Table 3-2 Hardware Resources (3 of 3)

Resource	Quantity	Description
I2C	Up to 11	Supports 7-bit and 10-bit addressing, up to 400 Kbit/s. Note: 1.8 V/3.3 V interfaces. Some pins are multiplexed.
SPI	Up to 5	Configurable for master/slave mode. Note: 1.8 V/3.3 V interfaces. Some pins are multiplexed.
CAN	Up to 2	Supports CAN-FD; supports 1 Mbps. Note: 1.8 V/3.3 V interfaces. Some pins are multiplexed.
PWM	Up to 3	3 independent PWM controllers supporting up to 16 PWM channels; 32-bit timers/counters. Note: 1.8 V/3.3 V interfaces. Some pins are multiplexed.

Remark: Some pins are multiplexed. Refer to the pin-function mapping table.

Translation note: The source labels the MIPI DCPHY row as CSI TX while its description states CSI RX. It also refers to eDP 3.1 in the DP row and states that eDP is multiplexed with the eDP controller. These descriptions are retained as supplied; confirm them with the manufacturer before hardware design.

Chapter 4 Development Resources

1. System-on-module pin definitions, editable carrier-board schematics, editable carrier-board PCB files and chip datasheets are provided to shorten the hardware design cycle.
2. System firmware images, kernel driver source code, filesystem source code and a wide range of demo programs are provided.
3. A complete platform development package and getting-started tutorials are provided to reduce software preparation time and simplify application development.
4. Detailed tutorials on communication in multi-core architectures are provided to address multi-core development bottlenecks.

Chapter 5 Electrical Characteristics

The operating environment is listed in Table 5-1.

Table 5-1 Operating Environment

Parameter	Minimum	Typical	Maximum
Operating Temperature	Commercial grade: 0°C	/	Commercial grade: 80°C
Operating Voltage	/	5 V	/

Power-consumption test results are listed in Table 5-2.

Table 5-2 Power Consumption

Parameter	Minimum	Typical	Maximum
Operating Temperature	Commercial grade: 0°C	/	Commercial grade: 80°C
Operating Power	1.38 W	/	3.83 W